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PEDR27V6466F-01-08

OKI Semiconductor

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MR27V6466F Preliminary

4,194,304-Word x 16-Bit or 2,097,152-Word x 32-Bit Synchronous One Time PROM

GENERAL DESCRIPTION

The MR27V6466F is a 64 Mbit One Time Programmable Synchronous Read Only Memory whose configuration can be electrically switched between 4,194,304 x 16 bit (word mode) and 2,097,152 x 32 bit (double word mode) by the state of the $\overline{WORD}$ pin. The MR27V6466F supports high speed synchronous read operation using a single 3.3 V power supply.

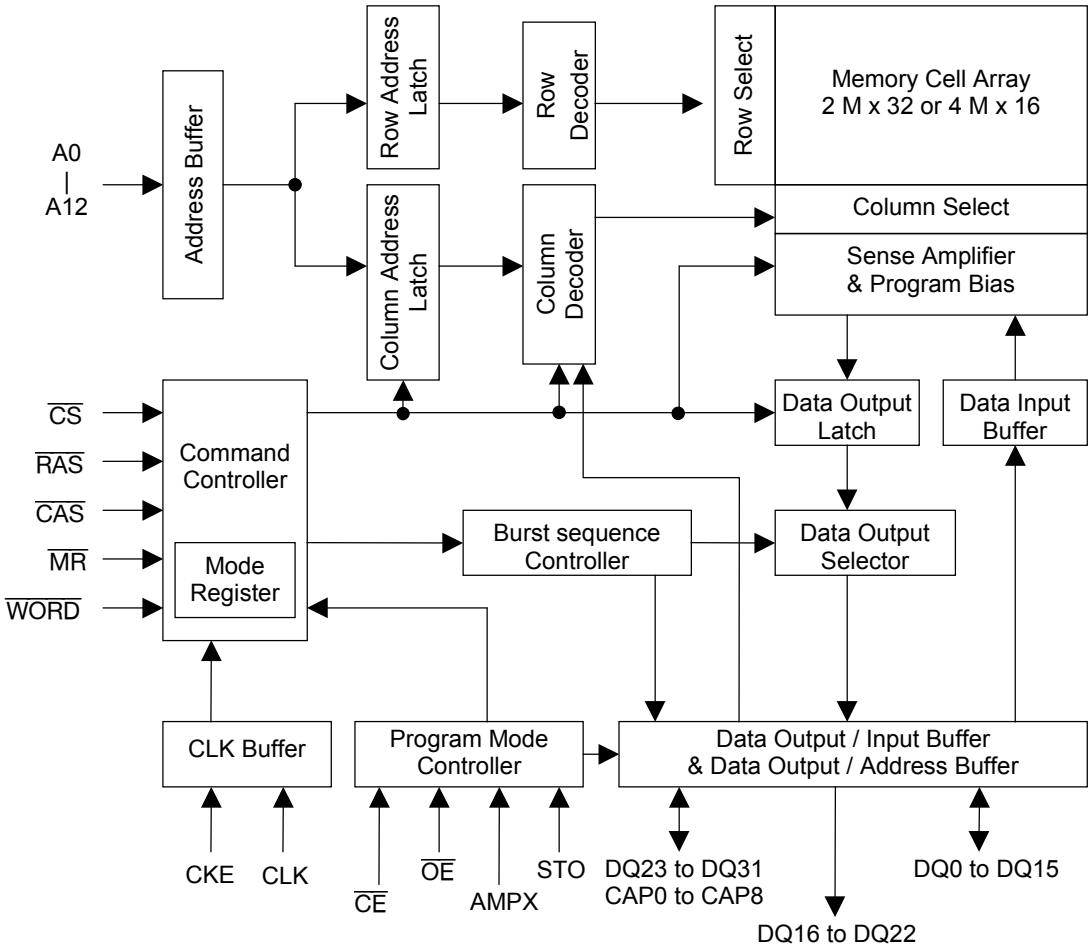
FEATURES ON READ

- 3.3 V power supply
- LVTTL compatible with multiplexed address
- Dual electrically switchable configuration
  4M x 16 (word mode) / 2M x 32 (double word mode)
- All inputs are sampled at the rising edge of the system clock.
- High speed read operation
  100 MHz : CAS Latency = 5, 6 tRCD min: 2 clock cycles
  66 MHz : CAS Latency = 5, 6 tRCD min: 2 clock cycles
  50 MHz : CAS Latency = 4, 5, 6 tRCD min: 1 clock cycles
  Burst length (4, 8)
  Data scramble (sequential, interleave)
- DQM for data out masking
- No Precharge operation is required. No Refresh operation is required.
- No power on sequence is required.
  Mode register is automatically initialized to the default state after power on.
  "Row Active" or "Mode Register Set" command is applicable as the first command just after power on.
- Single Bank operation
- Package: TSOP(2)86-P-400-0.50-K (Product Name : MR27V6466FTA)

FEATURES ON PROGRAMMING

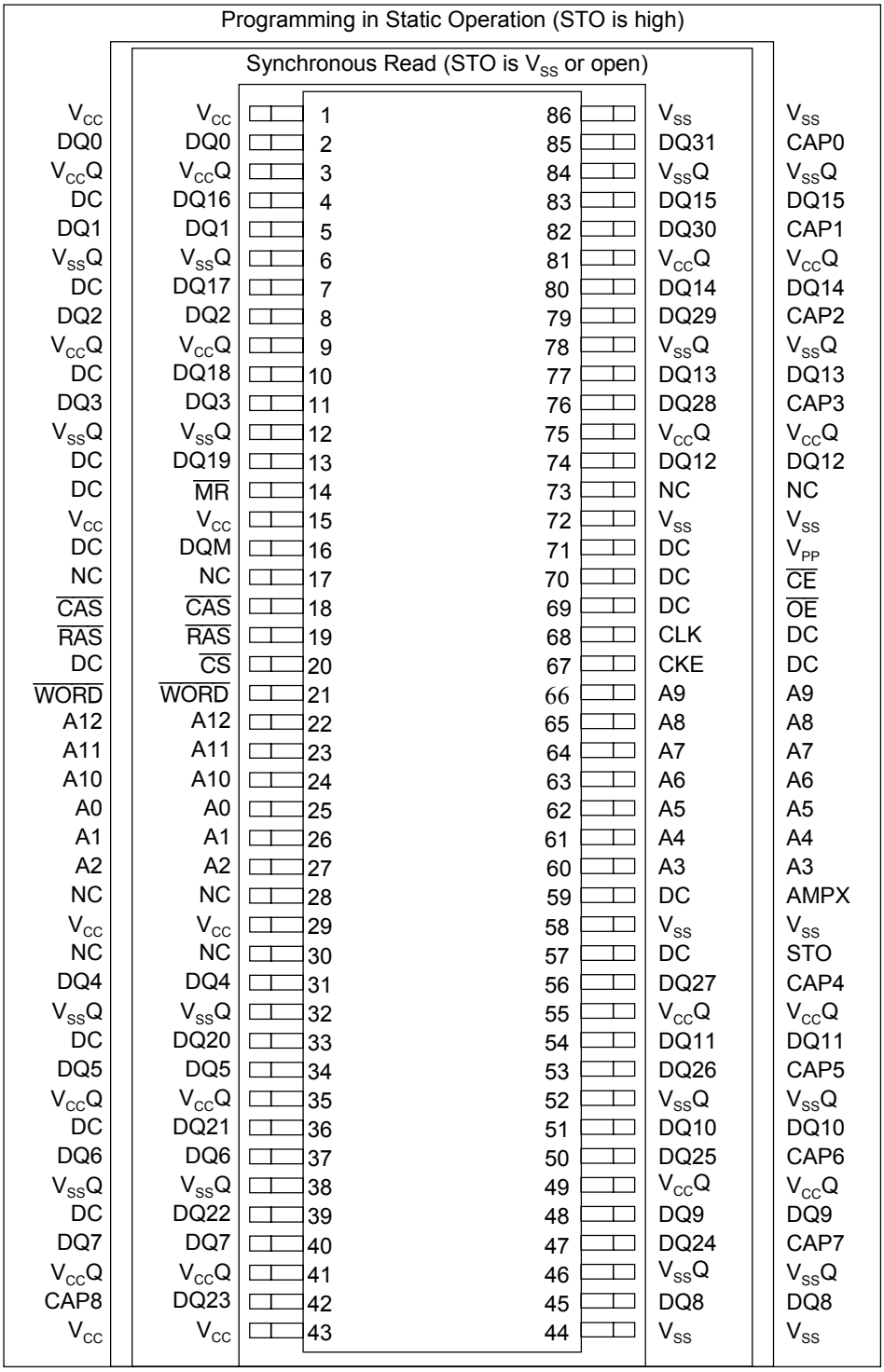
- 8.0 V programming power supply
- Programming algorithm is compatible with conventional asynchronous OTP.
  MR27V6466F can be programmed with conventional EPROM programmers.
  Synchronous Burst read or Static Programming Operation is selected by the state of STO pin.
  High STO level enables full static programming. (Program, Program Verify, Asynchronous Read)
  Low STO level enables synchronous burst read.
  Exclusive 86-pin socket adapters are available from OKI to support programming requirements.
  The socket adapter is used on a 48-DIP socket on the programmer.
  The socket adapter for 64M synchronous OTP is distinguished from the socket adapter for 32M SOTP.
  The socket adapter is designed with the STO pin connected to V_{CC} in order to program MR27V6466F as conventional OTP.
  EPROM programmer must have the algorithm for MR27V6466F on the exclusive socket adapter.
  *Device damage can occur if improper algorithm is used.
- Programming with address multiplexed input is also available.
- High speed programming
  25 μs programming pulse per word allows high speed programming.

BLOCK DIAGRAM



PIN CONFIGURATION

TOP VIEW


Programming in Static Operation (STO is high)
Synchronous Read (STO is VSS or open)
VCC VCC 1 86 VSS VSS
DQ0 DQ0 2 85 DQ31 CAP0
VCCQ VCCQ 3 84 VSSQ VSSQ
DC DQ16 4 83 DQ15 DQ15
DQ1 DQ1 5 82 DQ30 CAP1
VSSQ VSSQ 6 81 VCCQ VCCQ
DC DQ17 7 80 DQ14 DQ14
DQ2 DQ2 8 79 DQ29 CAP2
VCCQ VCCQ 9 78 VSSQ VSSQ
DC DQ18 10 77 DQ13 DQ13
DQ3 DQ3 11 76 DQ28 CAP3
VSSQ VSSQ 12 75 VCCQ VCCQ
DC DQ19 13 74 DQ12 DQ12
DC MR 14 73 NC NC
VCC VCC 15 72 VSS VSS
DC DQM 16 71 DC VPP
NC NC 17 70 DC CE
CAS CAS 18 69 DC OE
RAS RAS 19 68 CLK DC
DC CS 20 67 CKE DC
WORD WORD 21 66 A9 A9
A12 A12 22 65 A8 A8
A11 A11 23 64 A7 A7
A10 A10 24 63 A6 A6
A0 A0 25 62 A5 A5
A1 A1 26 61 A4 A4
A2 A2 27 60 A3 A3
NC NC 28 59 DC AMPX
VCC VCC 29 58 VSS VSS
NC NC 30 57 DC STO
DQ4 DQ4 31 56 DQ27 CAP4
VSSQ VSSQ 32 55 VCCQ VCCQ
DC DQ20 33 54 DQ11 DQ11
DQ5 DQ5 34 53 DQ26 CAP5
VCCQ VCCQ 35 52 VSSQ VSSQ
DC DQ21 36 51 DQ10 DQ10
DQ6 DQ6 37 50 DQ25 CAP6
VSSQ VSSQ 38 49 VCCQ VCCQ
DC DQ22 39 48 DQ9 DQ9
DQ7 DQ7 40 47 DQ24 CAP7
VCCQ VCCQ 41 46 VSSQ VSSQ
CAP8 DQ23 42 45 DQ8 DQ8
VCC VCC 43 44 VSS VSS

DC (Don't Care) : Logical input level is ignored. However the pin is connected to the input buffer of OTP.

PIN FUNCTION FOR SYNCHRONOUS READ OPERATION

(STO pin is low level or open)

Pin Name	Function	Description
STO	Static Operation	Must be low for synchronous operation. Internal resistance (around 10k ohms) pulls the input level down to V_{SS} when this pin is open. High level STO enables programming operation compatible with standard OTPs.
CLK	System Clock	All inputs are sampled at the rising edge.
$\overline{CS}$	Chip Select	Enables command sampling by the CLK signal with a low level on the $\overline{CS}$ input.
CKE	Clock Enable	Masks internal system clock to freeze the CLK operation of subsequent CLK cycle. CKE must be enabled for command sampling cycles. CLK is disabled for two types of operations. 1) Clock Suspend 2) Power Down
A0 to A12	Address	Row and column addresses are multiplexed on the same pins. Row address: RA0 to RA12 Column address: CA0 to CA7 (x32) /CA0 to CA8 (x16) LSB:CA0(Both x32 and x16)
$\overline{RAS}$	Row Address Strobe	Functionality depends on the combination. See the function table.
$\overline{CAS}$	Column Address Strobe	
$\overline{MR}$	Mode Register Set	
DQ0 to DQ31	Data Output	Data outputs are valid at the rising edge of CLK for read cycles. Except for read cycles DQn is high-Z state.
DQM	Data Output Masking	Data outputs are masked after two cycles from when high level DQM is applied.
$\overline{WORD}$	x32/x16 Organization Selection	The $\overline{WORD}$ pin defines the organization of each read command to be x16 (word mode) or x32 (double word mode). High = x32 Low = x16 When $\overline{WORD}$ is low (x16,word mode) ,DQ16 to DQ31 are held on High-Z state.
V_{CC}	Power Supply	3.3 V Power supply
V_{SS}	Ground	
$V_{CC}Q$	Data Output Power Supply	3.3 V Power supply to DQ0-DQ31
$V_{SS}Q$	Data Output Ground	
NC	No Connection	
DC	Don't Care	Logical input level is ignored.

PIN FUNCTION FOR PROGRAMMING OPERATION

(STO pin is high level)

Pin Name	Function	Description
STO	Static Operation	Must be set high for programming operation. Internal resistance (around 10 k ohms) pulls the input level down to V_{SS} for open state condition to be low level for synchronous read operation.
AMPX	Address Multiplex	When AMPX is low, the addresses are not multiplexed and all address bits must be supplied to A0 to A12 (Row Address) and CAP0 to CAP8 (Column Address) simultaneously. When AMPX is high, multiplexed address inputs are enabled on A0 to A12.
A0 to A12	Address	Row address input.
$\overline{RAS}$	Row Address Strobe	When AMPX is high, row address is latched at the rising egde of $\overline{RAS}$. When AMPX is low, input is not used.
$\overline{CAS}$	Column Address Atrobe	When AMPX is high, column address is latched at the rising egde of $\overline{CAS}$. When AMPX is low, input is not used.
DQ0 to DQ15	Data Input/Output	Input of data for programming and output for program verify and read data.
$\overline{WORD}$	x32/x16 Organization Selection	The $\overline{WORD}$ pin defines the organization to be x16 (word mode) or x32 (double word mode). High = x32 Low = x16 This pin must be set low for programming operation.
CAP0 to CAP8	Address Input	When $\overline{WORD}$ is low, High-Z state on CAP0 to CAP8 is held to be input pins. When AMPX is low, column address input. When AMPX is high, input is not used.
$\overline{OE}$	Output Enable	Control signal input for programming. $\overline{OE}$ of conventional OTPs.
$\overline{CE}$	Chip Enable	Control signal input for programming. Function for programming is associated with conventional OTPs.
V_{CC}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
$V_{CC}Q/V_{SS}Q$	Data Output Power/Ground	Power and ground for output.
V_{pp}	Program Power Supply	High voltage program power is supplied through V_{PP} pin. When V_{PP} is higher than a predetermined voltage level between V_{CC} + 0.5 V and V_{CC} + 2 V, pin function alters to high V_{PP} mode. To keep stable static read operation V_{PP} pin must be kept lower than V_{CC} + 0.5 V.

The persons who design socket adapter or make programming algorithm on the condition of omitting socket adapter provided with OKI study this table. Other persons can ignore this table.
The functionality of programming must be checked with the specification of socket adapter that will be supplied by OKI. MR27V6466F on the socket adapter is the same programming functionality as conventional OTPs.

FUNCTION COMMAND TABLE FOR SYNCHRONOUS READ

Command Name	Function	CKE_{N-1}	CKE_N	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	DQM	Add.	$\overline{WORD}$	STO	Note
Mode Register Set	Mode Register Set	H	X	L	L	L	L	X	Code	X	L	1
Row Active	Row Address Latch	H	X	L	L	H	H	X	RA	X	L	2
Read Word (x16)	Column Address Latch Trigger Burst Read	H	X	L	H	L	H	X	CA	L	L	3
Read Double Word (x32)	Column Address Latch Trigger Burst Read	H	X	L	H	L	H	X	CA	H	L	3
Burst Stop	Burst Stop	H	X	L	H	H	L	X	X	X	L	4
Precharge	Burst Stop	H	X	L	L	H	L	X	X	X	L	4
Clock Suspend (on Read)	Entry	H	L	H	X	X	X	X	X	X	L	5
	Exit	L	H	X	X	X	X	X	X	X	L	5
Power Down (on Active Standby)	Entry	H	L	H	X	X	X	X	X	X	L	6
	Exit	L	H	X	X	X	X	X	X	X	L	6
Read Output	Output Enable	H	X	X	X	X	X	L	X	X	L	
Mask Output	High-Z Output	H	X	X	X	X	X	H	X	X	L	
No Operation	Write on SDRAM	H	X	L	H	L	L	X	X	X	L	
	Illegal on SDRAM	H	H	L	L	L	H	X	X	X	L	
		H	X	H	X	X	X	X	X	X	L	
		H	X	L	H	H	H	X	X	X	L	

(H = Logical high, L = Logical low, X = Don't Care, L of STO includes pin open due to internal pull down resistor)
(CKE_N expresses the logical level at the simultaneous cycle with a command.)

Notes:

1. Refer to "Mode Register Field Table" for Address Codes, and Mode Transition Chart for operational state. After power on, any command can be sampled at any cycle in Active Standby state. After "Mode Register Set" command is sampled, no new command can be accepted for 3 CLK cycles. The $\overline{CS}$ input must be kept high for the 3 CLK cycles to prevent unexpected sampling of a command.
2. The "Row Active" command is effective till new "Row Active" command is implemented.
3. The $\overline{WORD}$ input is sampled simultaneously with "Read" command to select data width. A Double Word Burst (x32) or a Word Burst (x16) is selected by the $\overline{WORD}$ input for each "Read" command. On condition of constant voltage level on $\overline{WORD}$ pin, the organization is fixed to either x16 or x32. "Read" command ends it's implementation by itself at the finishing cycle of the burst read.
4. Since OTP technology uses static sense amplifiers, the "Precharge" command is not required. However, due to customer request for the similarity of logical input code with SDRAM command, the name of "Precharge" is adopted. The function of "Precharge" command and "Burst Stop" command is only to stop the burst read cycles delayed by CAS Latency.
5. Sampled low level CKE disables CLK buffer to suspend internal clock signals at the next rising edge of CLK. Sampled high level CKE enables internal clock at the next rising edge of CLK.
   Low level CKE sampled in the period from the simultaneous cycle with a "Read" command till the end of the burst read cycle is distinguished with internal command controller from the low level CKE sampled in Active Standby state, then power is consumed because of data sensing and burst read operation.
6. Low level CKE sampled in Active Standby state cuts power dissipation to be in Power Down state. High level CKE sampled in Power Down state enables internal CKE to be in Active Standby state with preserved row address.

FUNCTION STATE TABLE FOR SYNCHRONOUS READ

Current State	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{MR}$	Add.	Command	Action at next clock cycle or cycles	State after the completion of the command	Note
Active Standby	H	L	L	L	L	Code	Mode Register Set	Mode Register Set	Active Standby	
	H	L	L	H	H	RA	Row Active	Row Address Latch	Active Standby	1
	H	L	H	L	H	CA	Read	Column Address Latch Trigger Burst Read	Active Standby after Burst Read	
	L	H	X	X	X	X	Power Down	Entry Power Down	Power Down	2
	H	L	H	H	L	X	Burst Stop	NOP	Active Standby	
	H	L	L	H	L	X	Precharge	NOP	Active Standby	
	H	L	L	L	H	X	NOP	NOP	Active Standby	
	H	L	H	L	L	X	NOP	NOP	Active Standby	
	H	L	H	H	H	X	NOP	NOP	Active Standby	
	H	H	X	X	X	X	NOP	NOP	Active Standby	
Read	H	L	L	L	L	Code	Mode Register Set	Illegal		
	H	L	L	H	H	RA	Row Active	Row Address Latch	Active Standby	3
	H	L	H	L	H	CA	Read	Column Address Latch Trigger Burst Read	Active Standby after Burst Read	4
	L	X	X	X	X	X	Clock Suspend	Clock Suspend Entry	Clock Suspend	5
	H	L	H	H	L	X	Burst Stop	Stop the Burst Read Cycle delayed by CAS Latency	Active Standby	
	H	L	L	H	L	X	Precharge	Stop the Burst Read Cycle delayed by CAS Latency	Active Standby	
	H	L	L	L	H	X	NOP	NOP	Read	
	H	L	H	L	L	X	NOP	NOP	Read	
	H	L	H	H	H	X	NOP	NOP	Read	
	H	H	X	X	X	X	NOP	NOP	Read	
Power Down	H	X	X	X	X	X	Exit Power Down	Exit Power Down	Active Standby	2
	L	X	X	X	X	X	Power Down	Power Down	Power Down	2
Clock Suspend	H	X	X	X	X	X	Exit Clock Suspend	Exit Clock Suspend	Read	5
	L	X	X	X	X	X	Clock Suspend	Clock Suspend	Clock Suspend	5

(H = Logical high, L = Logical low, X = Don't Care)

Notes:

1. The latched row address is preserved during any state except another “Row Active” command.
2. Low level CKE sampled in Active Standby state disables internal clock and cuts power dissipation to be in Power Down state. High level CKE sampled in Power Down state enables internal clock to be in Active Standby state.
3. To preserve previous “Read” command, the latest “Row Active” command must be implemented at CL-1 clock cycle or later after the previous “Read” command.
4. To preserve previous “Read” command, the latest “Read” command must be implemented at CL-1 clock cycle or later after the previous “Read” command.
5. Sampled low level CKE in the period of Burst Read disables CLK buffer to suspend internal clock signals at the next rising edge of CLK. Sampled high level CKE in the Clock Suspend enables internal clock at the next rising edge of CLK.

MODE REGISTER FIELD TABLE

Address	A5	A4	A3	A2	A1	A0
Function	CAS Latency			Burst Type	Burst Length	

A5	A4	A3	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

A2	Type
0	Sequential
1	Interleave

A1	A0	Burst Length
0	0	Reserved
0	1	4
1	0	8
1	1	Reserved

Note:
A7 and A8 must be low during Mode Register Set cycle.
During power on, mode register is initialized to the default state when V_{CC} reaches a specific voltage (less than 3.0 V).
The default state of Mode Register is as shown below.

CAS Latency = 5
Burst Type = Sequential
Burst Length = 4

BURST SEQUENCE (BURST LENGTH = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

ADDRESSING MAP

(1) $\overline{\text{WORD}}$ = "H": x32 Organization

Pin Name	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Row Address	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Column Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	X	X	X	X	X

(X = Don't Care)

(2) $\overline{\text{WORD}}$ = "L": x16 Organization

Pin Name	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Row Address	RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Column Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	X	X	X	X

(X = Don't Care)

(3) Programming

Address displayed on programmer: x16	Ad0	Ad1	Ad2	Ad3	Ad4	Ad5	Ad6	Ad7	Ad8	Ad9	Ad10	Ad11	Ad12
Device Address: x16 STO = "H", AMPX = "L"	CAP0	CAP1	CAP2	CAP3	CAP4	CAP5	CAP6	CAP7	CAP8	A0	A1	A2	A3
Address (STO = "L") $\overline{\text{WORD}}$ = "L": x16	CA0	Note2 CA1	Note3 CA2	CA3	CA4	CA5	CA6	CA7	CA8	RA0	RA1	RA2	RA3
Address (STO = "L") $\overline{\text{WORD}}$ = "H": x32	Note1	CA0	Note4 CA1	Note5 CA2	CA3	CA4	CA5	CA6	CA7	RA0	RA1	RA2	RA3

Address displayed on programmer: x16	Ad13	Ad14	Ad15	Ad16	Ad17	Ad18	Ad19	Ad20	Ad21
Device Address: x16 STO = "H", AMPX = "L"	A4	A5	A6	A7	A8	A9	A10	A11	A12
Address (STO = "L") $\overline{\text{WORD}}$ = "L": x16	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12
Address (STO = "L") $\overline{\text{WORD}}$ = "H": x32	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12

Users of MR27V6466F are recommended to study the relationship between "Address displayed on programmer" and "Address (STO = "L")" ignoring "Device Address: x16, STO = "H"".
The order of data on Synchronous Read operation (STO="L") is checked on this table.
"Device Address : x16, STO = "H"" will be utilized to design socket adapter on programmer or to check boards designed to mount blank OTP and program OTP on board.
OKI will supply a socket adapter to program MR27V6466F as conventional x16 standard OTP. The users and the venders of programmer who use the socket adapter can ignore "Device Address: x16, STO = "H"".
The persons who use 32Mbit SOTP and 64Mbit SOTP must be careful to distinguish the socket adapters for 64Mbit from one for 32Mbit. The difference is caused from the additional assignment of column address and 1 bit shift of row address on 64Mbit SOTP

Note

1. A0 in programmer distinguishes upper word (x16) or lower word (x16) of Double word (x32).
   On word (x16) organization the address of device corresponds to the address of programmer.
   On double word (x32) organization the address numeral code of device is half of that in programmer, and output on DQ0 to DQ15 is lower word (A0 = "0") and output on DQ16 to DQ31 is upper word (A0 = "1").
2. CA1 is MSB of burst read on condition of $\overline{\text{WORD}}$ = "L" and BL = 4.
3. CA2 is MSB of burst read on condition of $\overline{\text{WORD}}$ = "L" and BL = 8.
4. CA1 is MSB of burst read on condition of $\overline{\text{WORD}}$ = "H" and BL = 4.
5. CA2 is MSB of burst read on condition of $\overline{\text{WORD}}$ = "H" and BL = 8.

READ OPERATIONS

Clock (CLK)

The clock input enables MR27V6466F to sample all the inputs, to control internal circuitry, and to turn on output drivers. All timings are referred to the rising edge of the clock. All inputs with high level CKE and low level $\overline{CS}$ should be valid at the rising edge of CLK for proper functionality.

Clock Enable (CKE)

The clock enable (CKE) turns on or switches off the admission of the clock input into the internal clock signal lines. All internal circuits are controlled by the internal clock signal to implement each command. High level CKE sampled at CKE_{N-1} clock cycle enables the admission of the rising edge of clock input into internal clock line at CKE_N cycle. Low level CKE sampled at CKE_{N-1} cycle suspends the rising edge of CLK at CKE_N cycle. The suspension of internal clock signal in all state ignores new input except CKE, and holds internal state and output state. Low level CKE in Active Standby state, defined as Power Down state, cuts power dissipation. In Power Down state, the contents of mode resister and Row Address are preserved. After recovering high level CKE to exit from Power Down state, MR27V6466F is in Active Standby state. Low level CKE just after the sampling of "Read" command till the completion of burst read, defined as Clock Suspend, makes read operation go on with power dissipation. Any command operation does not interrupted by arbitrary low level CKE. Sampling command with low level CKE preceded with high level CKE is illegal.

Power On

Apply power and start clock considering following issues.

1. During power on, Mode Register is initialized into the default state.
   (default state: CAS latency = 5, Burst Type = Sequential, Burst length = 4)
2. After power on, MR27V6466F is in Active Standby state and ready for "Mode Register set" command or "Row Active" command. MR27V6466F requires neither command nor waiting time as power on sequence after starting CLK input in order to start "Row Active" command to read data.
3. It is recommended in order to utilize default state of Mode Register that $\overline{MR}$ and CKE inputs are maintained to be pulled up during power on till the implementation of the first "Row Active" command. After above power on, "Row Active" command and "Read" command can be started immediately on default Mode Register state.
4. It is recommended that DQM input is maintained to be pulled up to prevent unexpected operation of output buffers.

Organization Control

The organization of data output (DQ0~DQ31) depends on the logical level on $\overline{WORD}$ at the input timing of each "Read" command. High level sampling of $\overline{WORD}$ derives double word mode (x32) output and low level sampling of $\overline{WORD}$ derives word mode (x16) output. Constant $\overline{WORD}$ level input brings consistent organization.

MODE Register

Mode register stores the operating mode of MR27V6466F. Operating modes are consisted with CAS latency, Burst Type and Burst Length. Registration of RAS latency is not required, because RAS to CAS delay (tRCD) is requested independently of system clock. When the contents of Mode register are required to be changed for the next operation, "Mode Register Set" command can be sampled at any cycle in Active Standby state. After "Mode Register Set" command is sampled, $\overline{CS}$ must be fixed to logical high level to prevent sampling of new command input during succeeding three clock cycles.
Refer to Mode Resister Field Table for the relation between Operation modes and input pin assignment

READ OPERATIONS

CAS Latency

After sampling "Read" command, MR27V6466F starts actual data read operation with sense amplifiers, and transmits the data from sense amplifiers to data out buffers to start burst read. This flow of sequential functionality takes time as clock cycles defined as CAS latency (CL). CAS latency can be set in Mode Register between from four cycles to six cycles. In this sequence (from sampling "Read" command to start of driving data bus), sense amplifiers consume maximum current flow. The detailed sequence is as shown below.

1. Fix the column address of memory matrix driver. Row address is already fixed with "Row Active" command. (at 1st cycle)

2. Read the data of selected memory cells with sense amplifiers.

3. Deliver the data detected with sense amplifiers to the register for data output latch.

4. Couple selectively the section of the register storing each (double) word to output buffers.

5. Enable the output buffers to drive data bus (at CL-1 cycle).

6. Data the output on data bus can be sampled at the rising edge of system clock at CL cycle.

New "Row Active" command or new "Read" command can be sampled to perform gapless burst read at CL-1 clock cycle of the last "Read" command. New command preceeding CL-1 cycle interrupts sense amplifiers to read the data at the selected memory cells of the last "Read" command. Interrupted "Read" command perishes or outputs invalid data before the starting of the data burst of new "Read" command. Refer to the timing chart of "Burst Read/Interrupt I" and "Burst Read/Interrupt II".

Burst Read

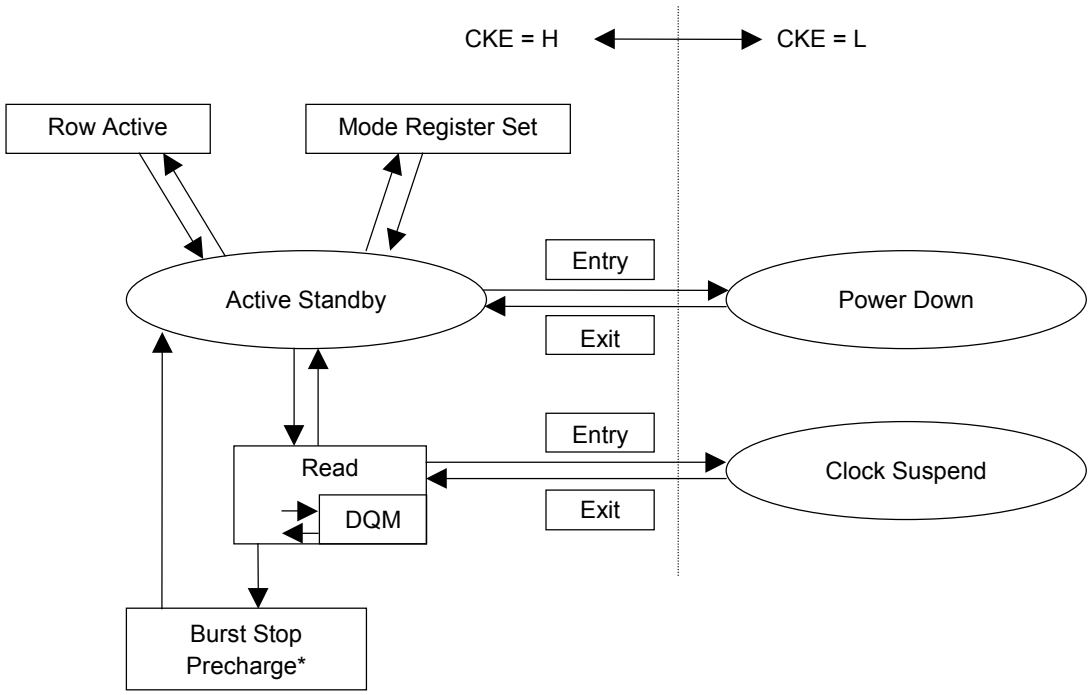
Data outputs are consecutive during the cycle number defined as Burst Length (BL). The latest burst read is completed unless any interruption such as "Precharge" command stops the sequential data output. Burst Length is set in Mode Register as either four or eight. After sampling of "Read" command, the first output can be read at the cycle delayed by CAS latency. Burst Type is also stored in Mode register as either sequential or interleave. The output buffers go into a high impedance state after burst read sequence is finished, unless a new "Read" command has been sampled to perform gapless read or preemptive read. Burst read can be interrupted by "Burst Stop" command or "Precharge" command at the cycle delayed by CAS latency from the command. On condition that reading data with sense amplifiers of preceding "Read" command is not interrupted by new "Read" command or "Row active" command, burst read of preceding "Read" command is continued regularly until the burst data sequence of the new "Read" command starts. The new (latest) burst data sequence always starts regularly.

DQM

Input level on DQM is sampled at the rising edge of system clock to mask data at two cycles later. The output of masked data is in a high-Z state.

Read Operation

Mode transfer chart



* All operation of “Precharge” command is to stop burst read.

Note:

: passing command

: state can be kept for any duration

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Voltage on V_{CC} Relative to V_{SS}	V_{CC}, $V_{CC}Q$	–0.5	5	V
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}, DC	–0.5	V_{CC} + 0.5	V
Voltage on V_{PP} Relative to V_{SS}	V_{PP}	–0.5	10	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	–55	125	°C
Short Circuit Current	I_{OS}	—	50	mA
Power Dissipation	P_D	—	1.0	W

RECOMMENDED OPERATION CONDITION FOR SYNCRONOUS READ

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}, $V_{CC}Q$	3.0	3.3	3.6	V	
Voltage Level on DC Pin	—	–0.5	—	V_{CC} + 0.3	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Operating Temperature	T_A	0	—	70	°C	
Power Dissipation1 (Airflow over 1 m/s)	P_{D1}	—	—	0.6	W	
Power Dissipation2 (No airflow)	P_{D2}	—	—	0.4	W	
Power Dissipation3 (Airflow over 1 m/s)	P_{D3}	—	—	0.9	W	3
Power Dissipation4 (No airflow)	P_{D4}	—	—	0.6	W	3

Notes:
1. V_{IH} max can be V_{CC} + 1.5V for the pulse width shorter than 3 ns.
   Pulse width is measured at 50% of pulse peak level.
2. V_{IL} min can be –1.5 V for the pulse width shorter than 3 ns.
   Pulse width is measured at 50% of pulse peak level.
3. The clock frequency is under 83MHz.

CAPACITANCE

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	5	pF
Output Capacitance	C_{OUT}	—	7	pF

DC CHARACTERISTICS FOR SYNCHRONOUS READ

Parameter	Symbol	Min.	Max.	Unit	Test Condition	
Power Down Current	I_{CCS1}	—	1	mA	CKE = 0.8V	tCC = 10 ns
	I_{CCS2}	—	150	μA	CKE = 0 V	
Active Standby Current	I_{CC1}	—	120	mA	CKE = 2.4V	$\overline{CS}$ = 2.4V tCC = 10 ns
Gapless Burst Read Current	I_{CC2}	—	250	mA	CKE = 2.4V	tCC = 10 ns, DQM = H, CL = 5, BL = 4
Input Leak Current	I_{IL}	–10	10	μA	0V > V_{IN} > V_{CC} + 0.3 V	
Output Leak Current	I_{OL}	–10	10	μA	0V > V_{IN} > V_{CC}	
Input High Voltage	V_{IH}	2.0	V_{CC}+0.3V	V	Note 1	
Input Low Voltage	V_{IL}	–0.3	0.8	V	Note 2	
Voltage Level on DC Pin		–0.5	V_{CC}+0.3V	V		
Output High Voltage Level	V_{OH}	2.4	—	V	I_{OH} = –4 mA	
Output Low Voltage Level	V_{OL}	—	0.4	V	I_{OL} = 4 mA	

(Voltage levels are referred to V_{SS})

Notes:
1. V_{IH} max can be V_{CC} + 1.5V for the pulse width shorter than 3 ns.
   Pulse width is measured at 50% of pulse peak level.
2. V_{IL} min can be –1.5 V for the pulse width shorter than 3 ns.
   Pulse width is measured at 50% of pulse peak level.

AC CHARACTERISTICS FOR SYNCHRONOUS READ (1/2)

Parameter			Symbol	Min.	Max.	Unit	Notes
CLK Cycle Time			tCC	10	—	ns	
Data to Valid Output Delay			tAC	—	6	ns	
Data Output Hold Time			tOH	2.3	—	ns	
CLK High Pulse Width			tCH	3	—	ns	
CLK Low Pulse Width			tCL	3	—	ns	
Input Setup Time			tSI	2	—	ns	
Input Hold Time			tHI	1	—	ns	
CLK to Output in Low-Z			tOLZ	0	—	ns	
CLK to Output in High-Z			tOHZ	—	7	ns	
Input Level Transition Time			tT	0.1	10	ns	
"Row Active" to "Read" Delay Time			tRCD	1CLK	—	Cycle	2
				2CLK	—	Cycle	
"Read" to "Row Active" Delay (Words of preceding "Read" command can be read) < Random Access >	BL = 4	CL = 4	tCRD	3CLK	—	Cycle	1,2
		CL = 5	tCRD	4CLK	—	Cycle	1
		CL = 6	tCRD	5CLK	—	Cycle	1
	BL = 8	CL = 4	tCRD	3CLK	—	Cycle	1,2
		CL = 5	tCRD	4CLK	—	Cycle	1
		CL = 6	tCRD	5CLK	—	Cycle	1
"Read" to "Read" Delay (Words of preceding "Read" command can be read) < Sequential Access >	BL = 4	CL = 4	tCCD	3CLK	—	Cycle	1,2
		CL = 5	tCCD	4CLK	—	Cycle	1
		CL = 6	tCCD	5CLK	—	Cycle	1
	BL = 8	CL = 4	tCCD	3CLK	—	Cycle	1,2
		CL = 5	tCCD	4CLK	—	Cycle	1
		CL = 6	tCCD	5CLK	—	Cycle	1
"Row Active" Cycle Time (Words of preceding "Read" command can be read) < Random Access >	BL = 4	CL = 4	tRC	3CLK + tRCD	—	Cycle	1,2
		CL = 5	tRC	4CLK + tRCD	—	Cycle	1
		CL = 6	tRC	5CLK + tRCD	—	Cycle	1
	BL = 8	CL = 4	tRC	3CLK + tRCD	—	Cycle	1,2
		CL = 5	tRC	4CLK + tRCD	—	Cycle	1
		CL = 6	tRC	5CLK + tRCD	—	Cycle	1
"Read" to "Read" Delay (Consecutive Column Read) < Sequential Access >	BL = 4	CL = 4	tCCD	4CLK	—	Cycle	1,2
		CL = 5	tCCD	4CLK	—	Cycle	1
	BL = 8	CL = 4	tCCD	8CLK	—	Cycle	1,2
		CL = 5	tCCD	8CLK	—	Cycle	1
		CL = 6	tCCD	8CLK	—	Cycle	1
"Read" to "Burst Stop" Delay				1CLK	—	Cycle	
"Read" to "Precharge" Delay				1CLK	—	Cycle	
Power down Exit Setup Time			tPDE	tSI + 1CLK	—	Cycle	
Power down Exit to "Read" Delay			tPDR	tSI + 3CLK	—	Cycle	

Notes:
1. The shortage of clock cycles interrupts the data sensing of preceding "Read" command.
   The shortage of cycle time for preceding command is detected by internal command controller to cease the preceding command operation.
   The latest "Row Active" or "Read" command is completed.
   When a legal tCCD is shorter than BL, burst read is terminated with another burst read.
2. Up to 50 MHz

AC CHARACTERISTICS FOR SYNCHRONOUS READ (2/2)

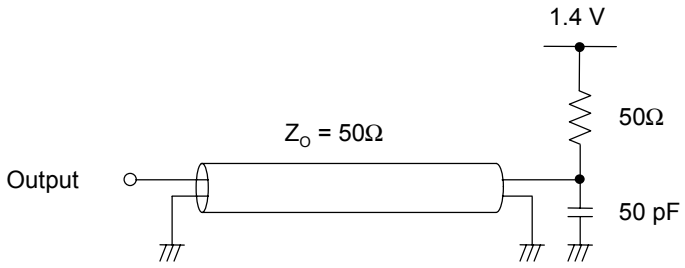
Parameter	Symbol	Value	Unit	Notes
Clock Disable Time from CKE	tCKE	1CLK	Cycle	
Clock Enable Time from CKE	tCKE	1CLK	Cycle	
Output High Impedance from DQM	tDQM	2CLK	Cycle	
Recovery from DQM	tDQM	2CLK	Cycle	
Output High Impedance from “Burst Stop”	tBOH	CL	Cycle	
Output High Impedance from “Precharge”	tPOH	CL	Cycle	
“Row Active” Input from “Mode Register Set”	tMRD	3	Cycle	

AC TEST CONDITIONS

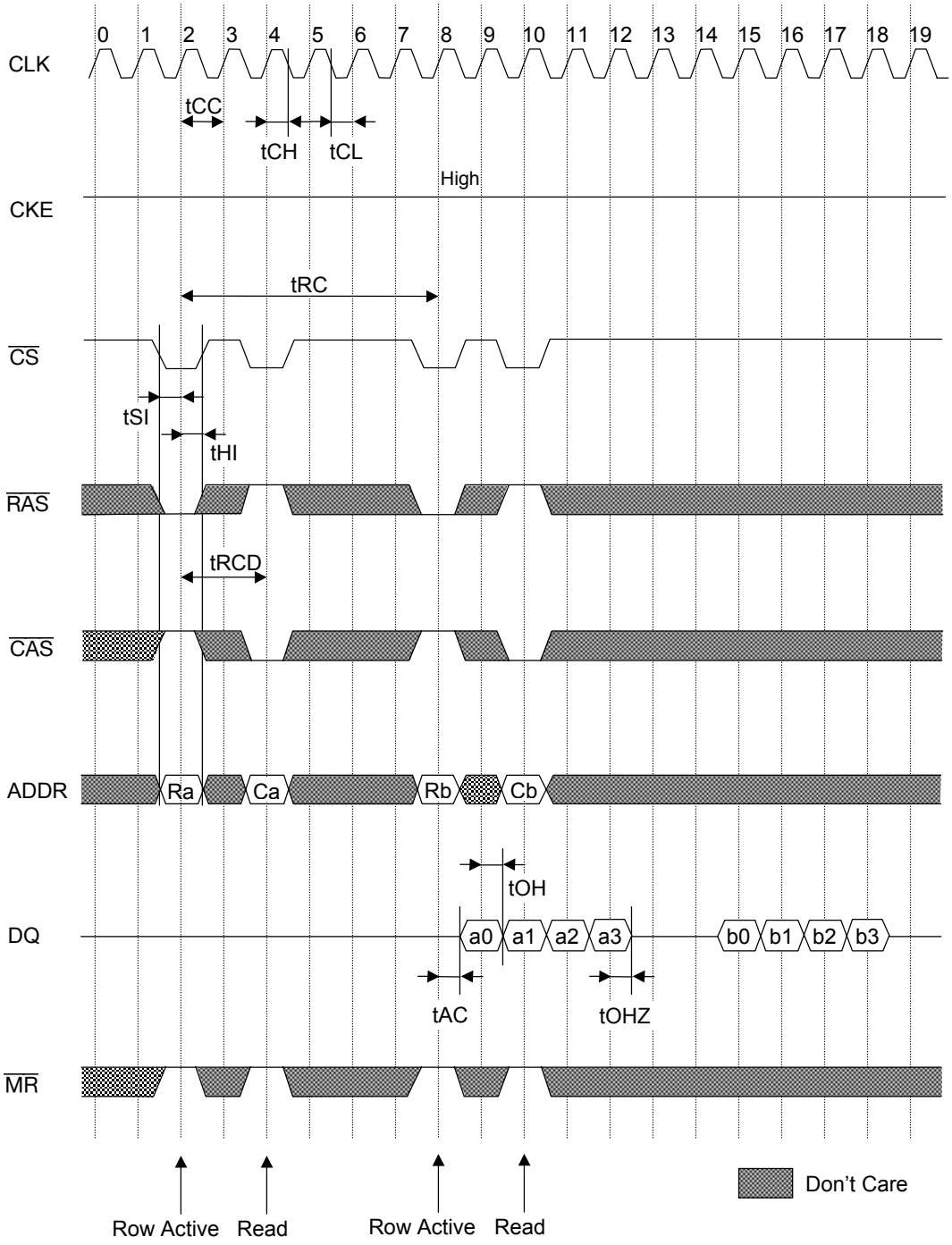
Parameter	Values	Notes
Input Signal Levels	V_{IH}/V_{IL} = 2.4 V/0.4 V	
Timing Reference Level of Input/Output Signals	1.4 V	
Transition Time of Input Signals	tr/tf = 1 ns/1 ns	1
Output Load	LVTTL	2

Notes:
1. The transition time of input signals is measured between 0.8 V and 2.0 V.
   If tr or tf is longer than 1ns, the "Timing Reference Level of Input/Output Signals" is changed to V_{IL} or V_{IH}/0.8 V or 2.0 V respectively.

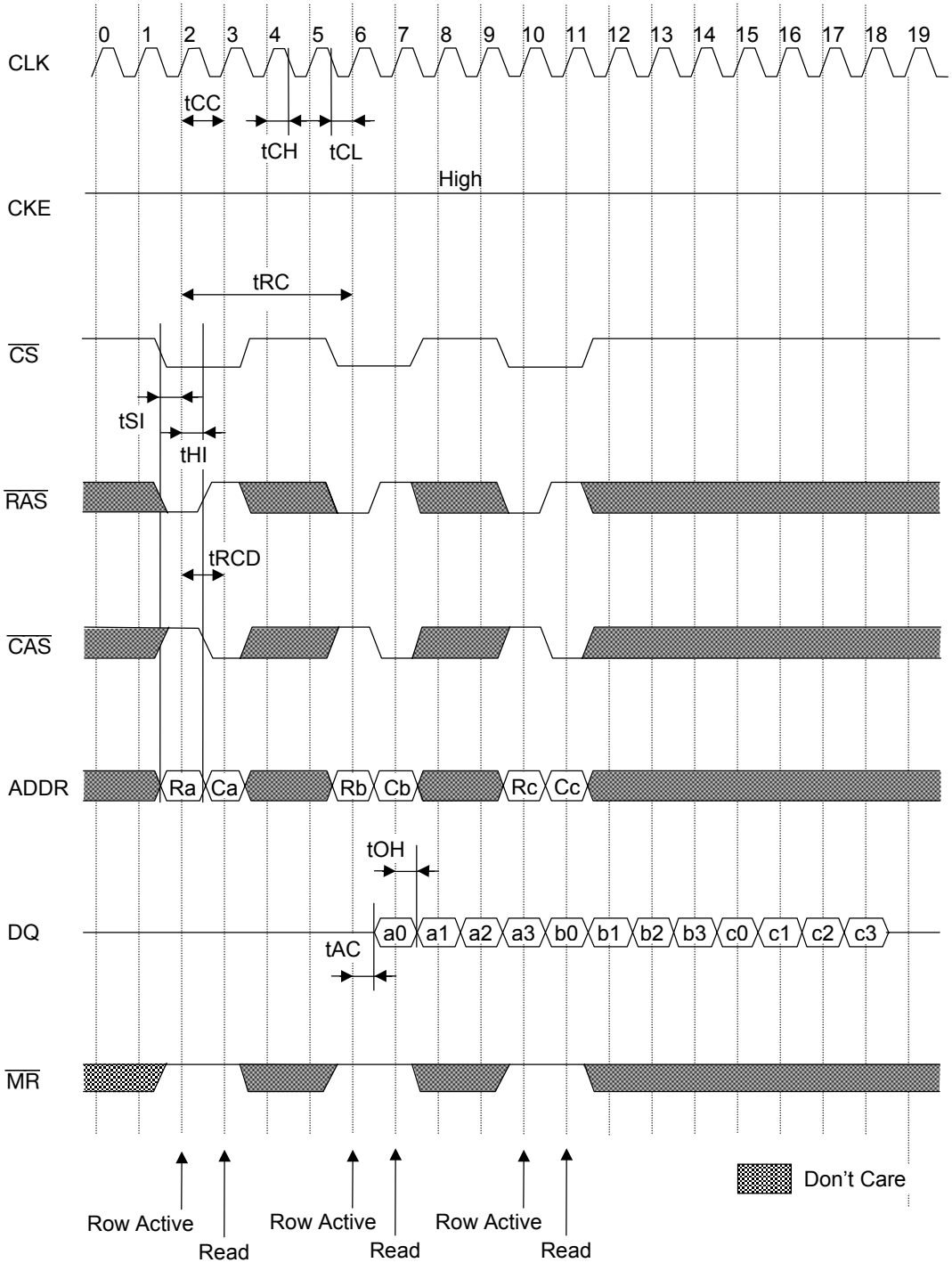
2. Output Load



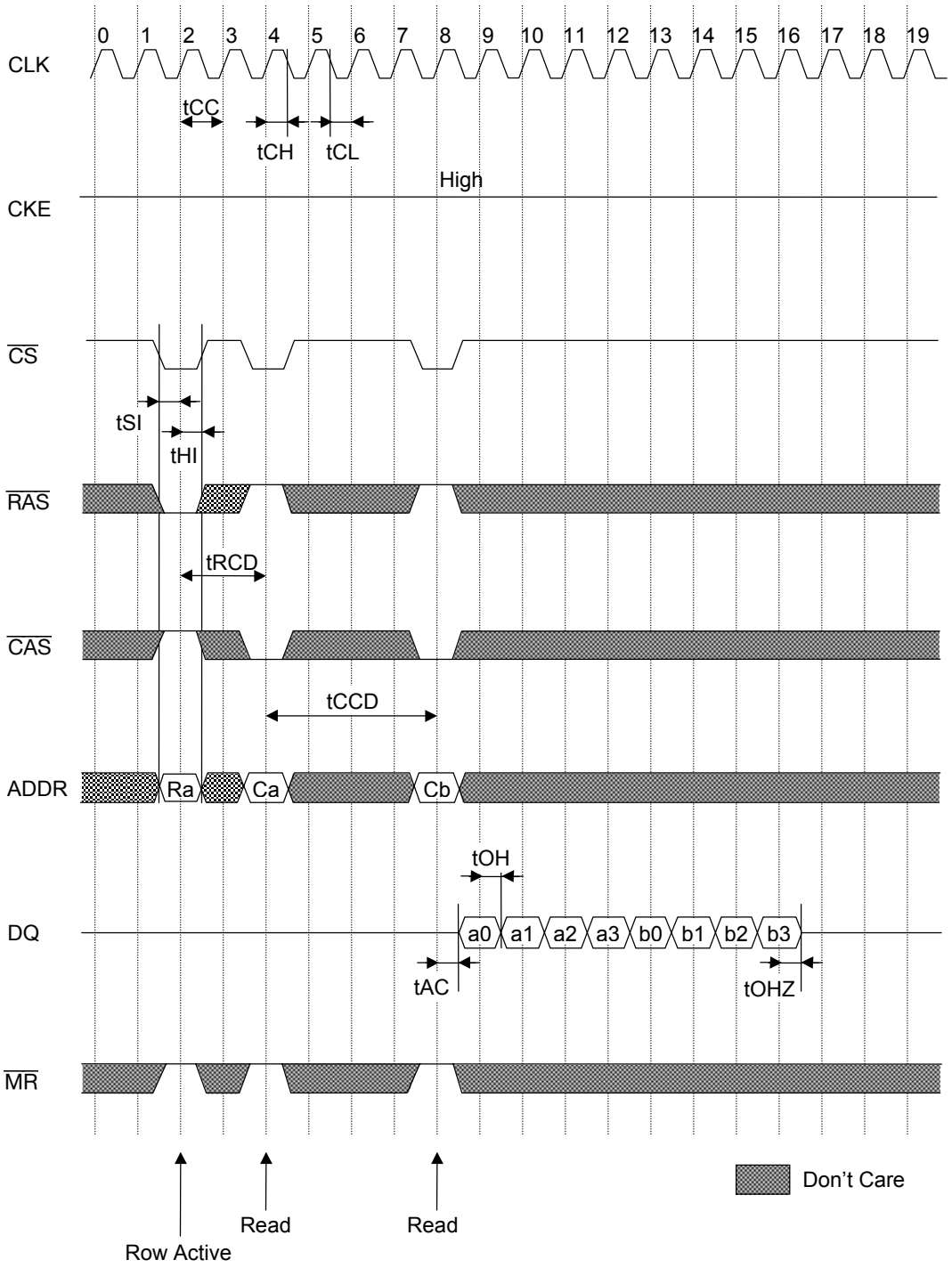
Read Cycle I: Random Access @ CAS Latency = 5, Burst length = 4



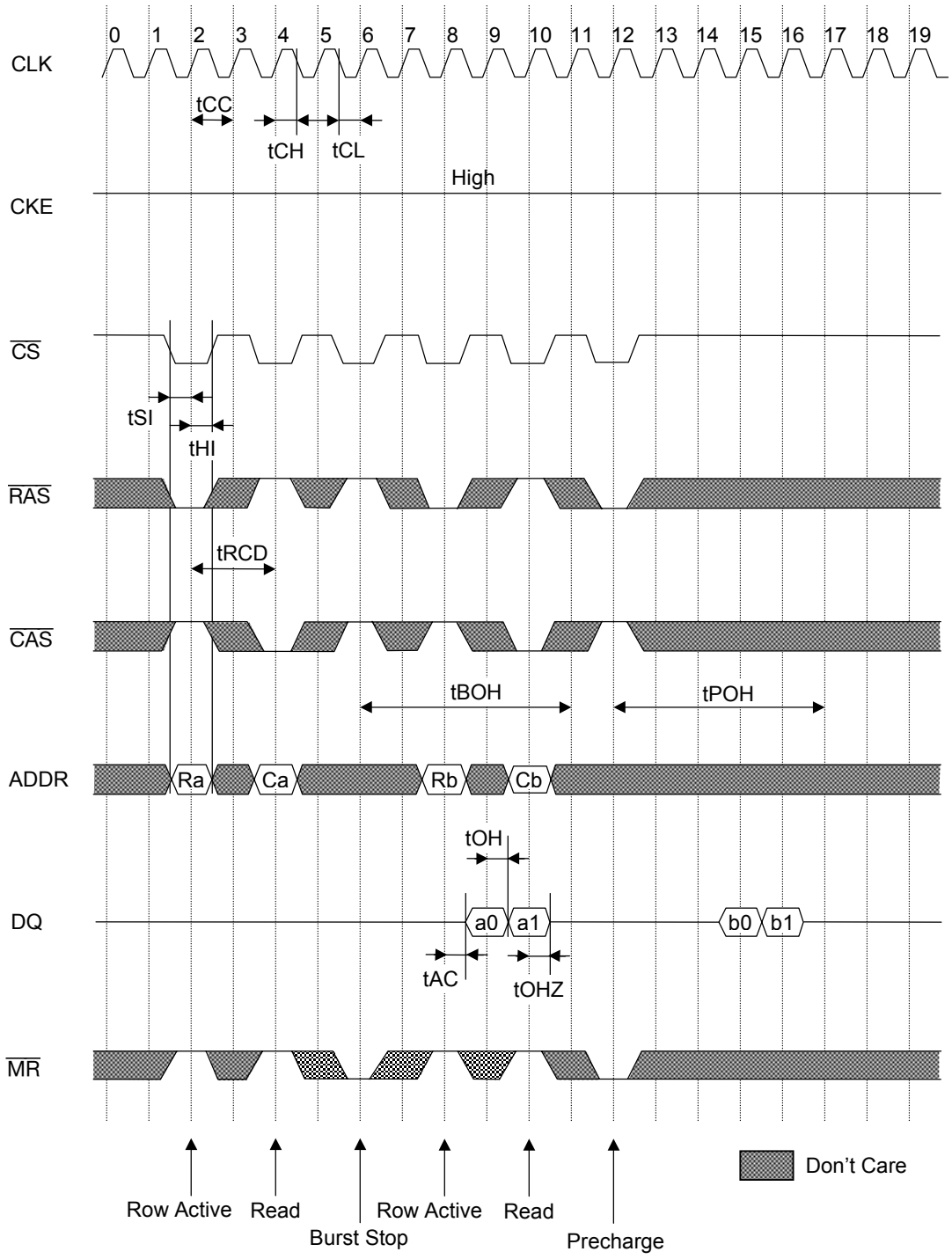
Read Cycle II: Random Access with Gapless Burst @ CAS Latency = 4, Burst length = 4



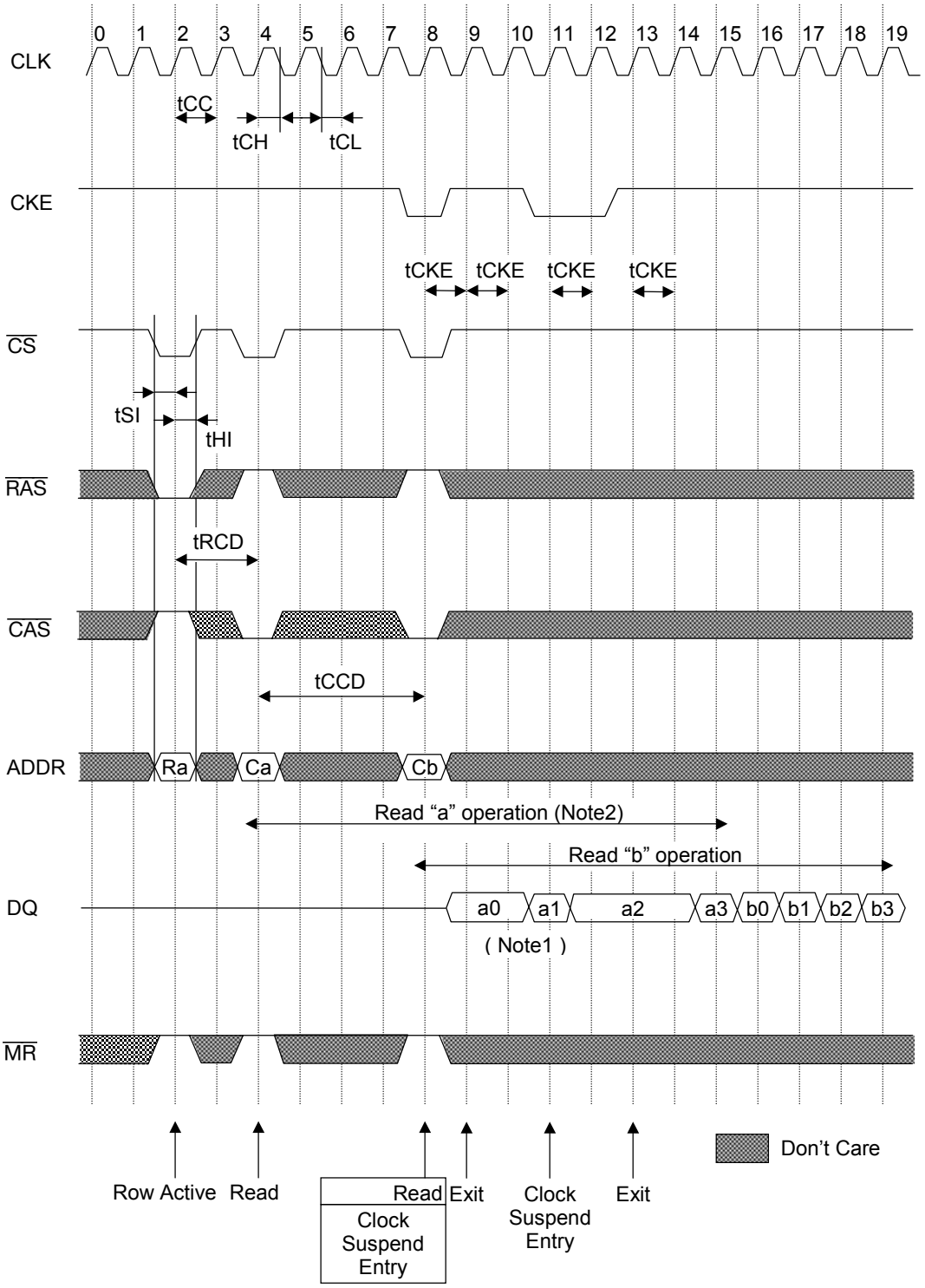
Read Cycle III: Consecutive Column Read @ CAS Latency = 5, Burst length = 4



"Burst Stop" command & "Precharge" command @ CAS Latency = 5



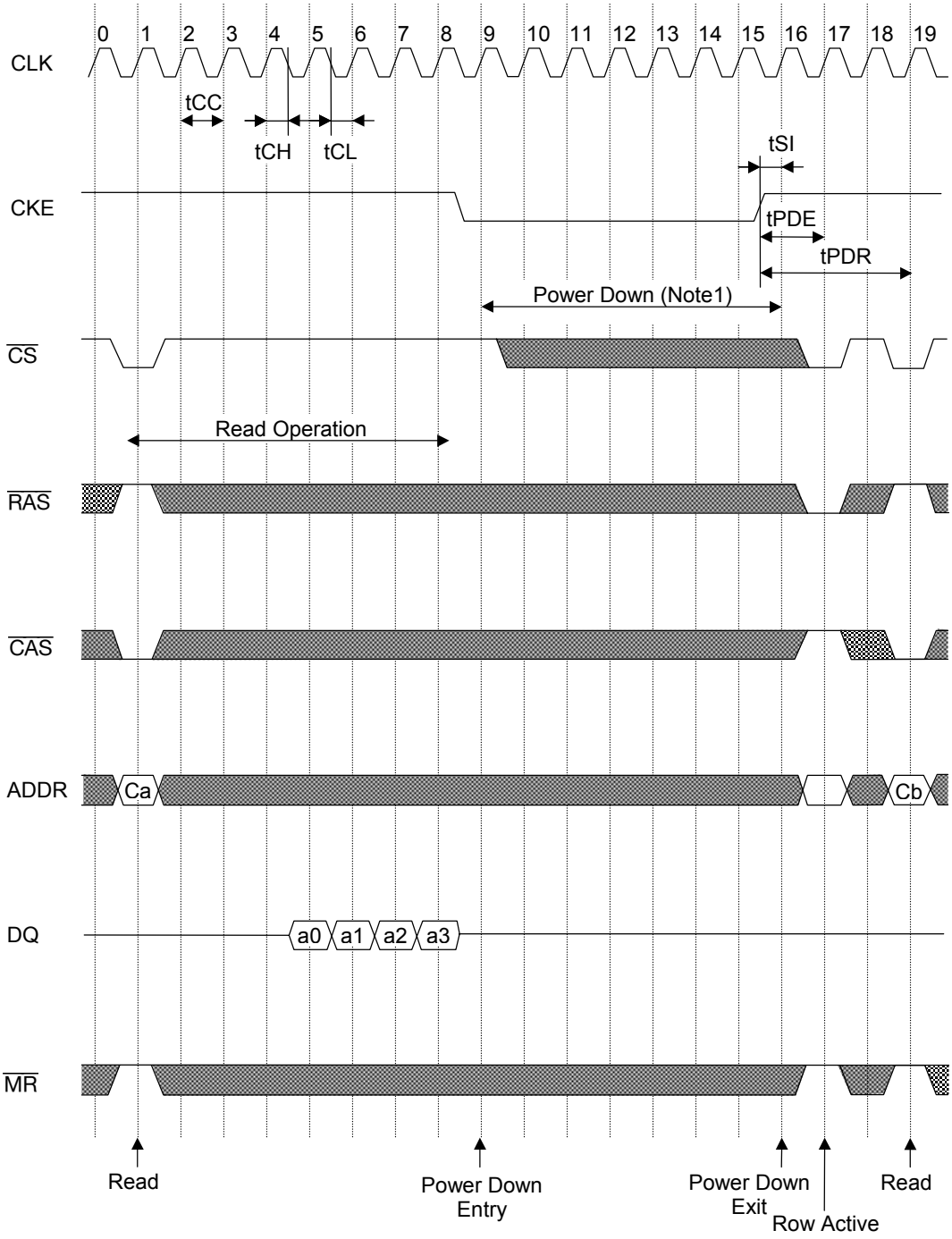
Clock Suspend @ CAS Latency = 5, Burst length = 4



Note

1. At cycle numbers 9, 12 and 13, the rising edge of internal clock is omitted because of low level CKE at cycles 8, 11 and 12.
2. Clock suspend is defined with the low level CKE sampled in the period of read operation.

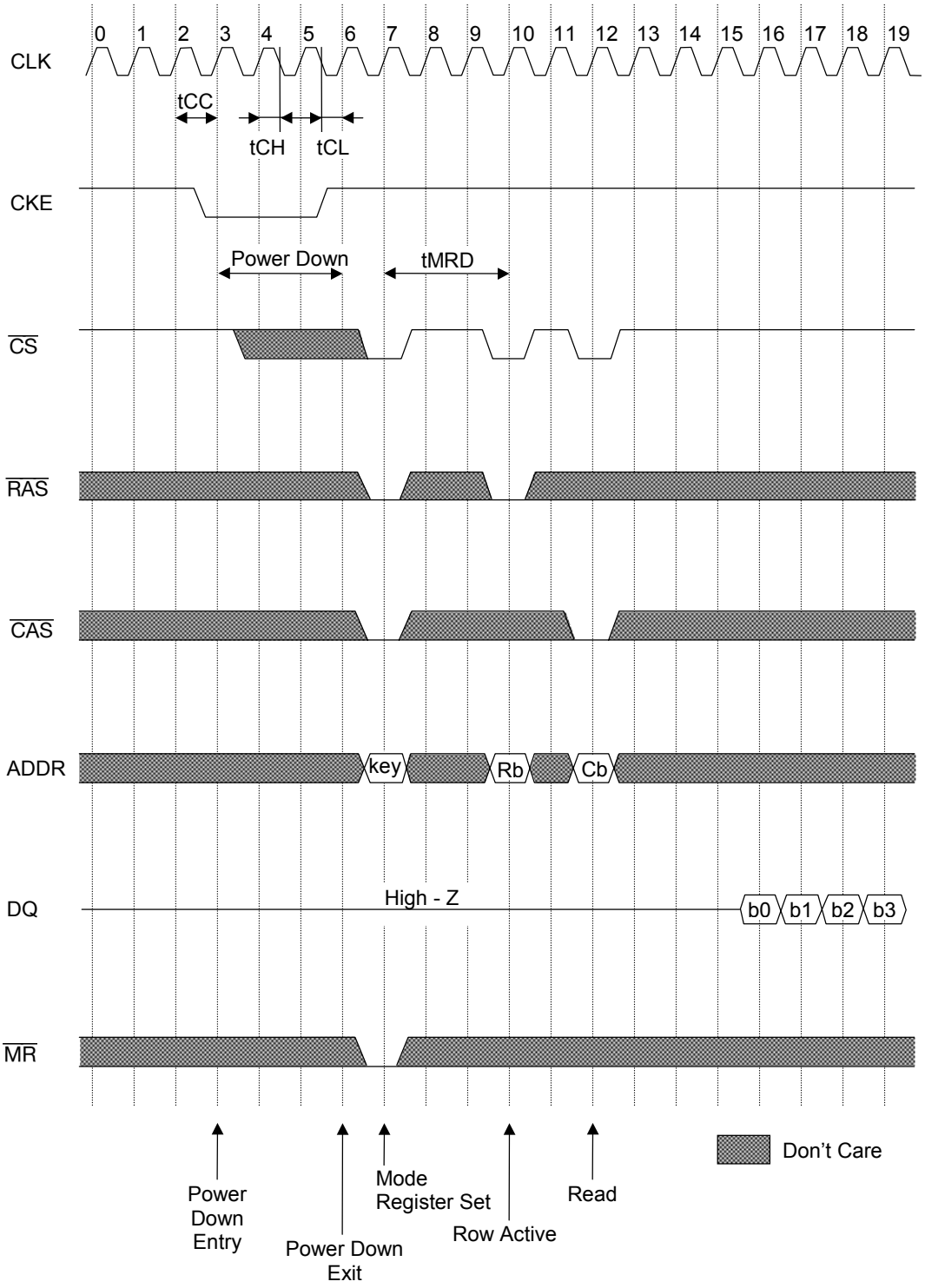
Power Down @ CAS Latency = 4, Burst length = 4



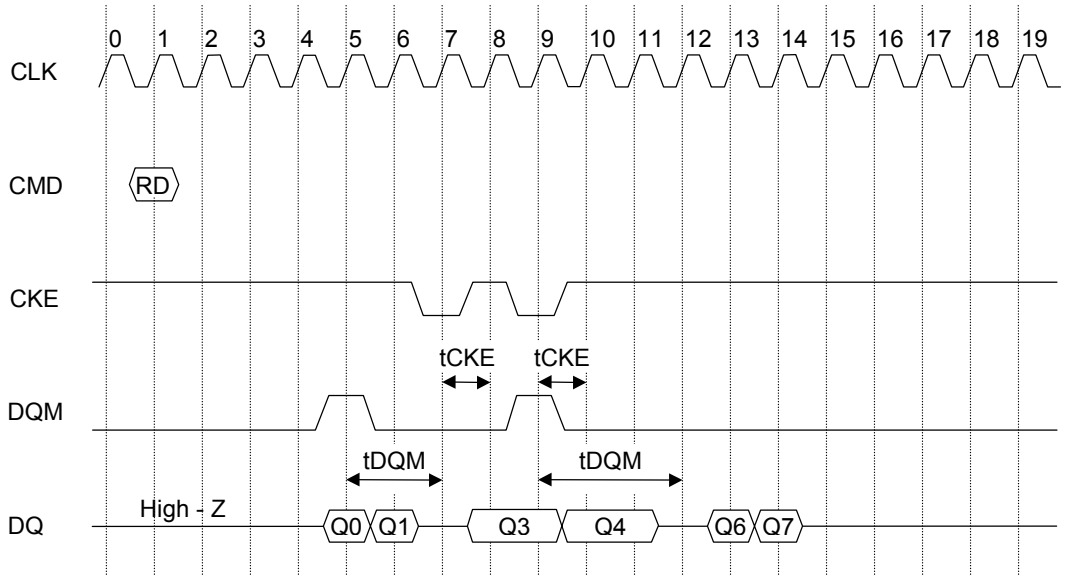
Note

1. Minimum current consumption is expected in Power Down state.
   Low level CKE sampled only in Active Standby state is defined as Power Down "Entry" command and it cuts current consumption into a minimum level.
   After Power Down "Exit" the contents of Mode Register and row address are preserved.
   During Power Down state no command can be sampled.

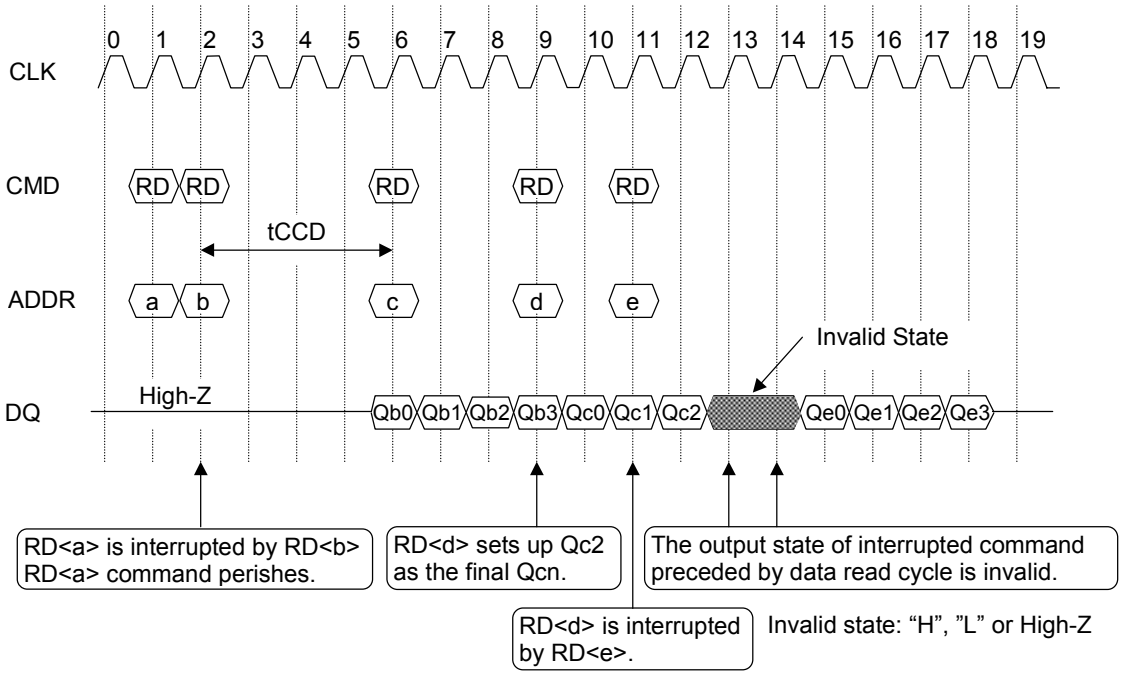
Mode Register Set @ CAS Latency = 4, Burst length = 4



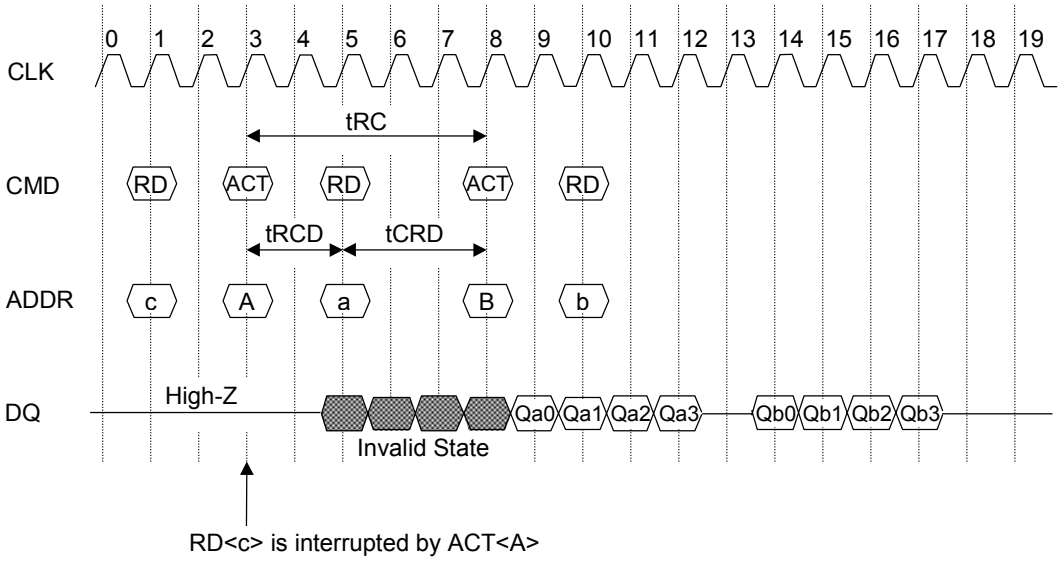
DQM Operation @ CAS Latency = 4, Burst length = 8



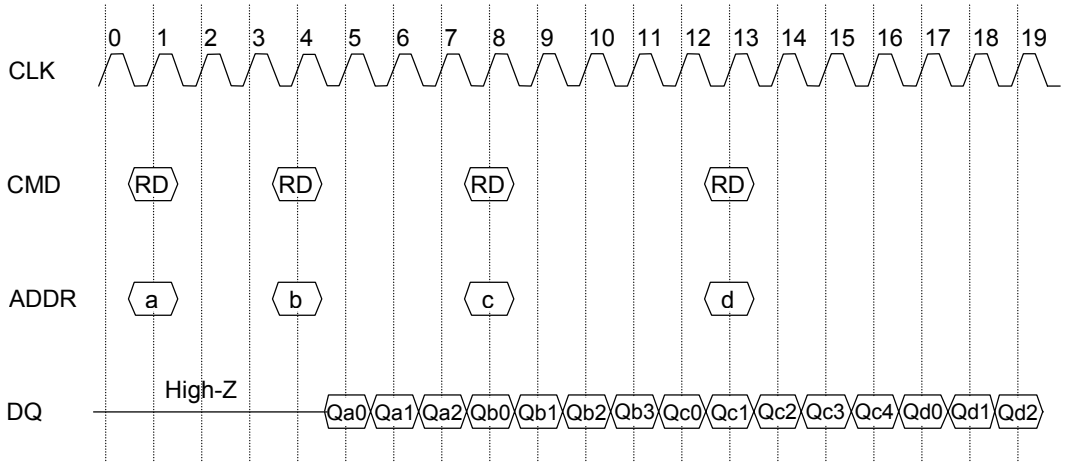
Burst Read/Interrupt I @ CAS Latency = 4, Burst length = 8


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
CLK
CMD
RD RD RD RD RD
tCCD
ADDR
a b c d e
Invalid State
DQ
High-Z
Qb0 Qb1 Qb2 Qb3 Qc0 Qc1 Qc2 Qe0 Qe1 Qe2 Qe3
RD<a> is interrupted by RD<b>
RD<a> command perishes.
RD<d> sets up Qc2
as the final Qcn.
The output state of interrupted command
preceded by data read cycle is invalid.
RD<d> is interrupted
by RD<e>.
Invalid state: “H”, ”L” or High-Z

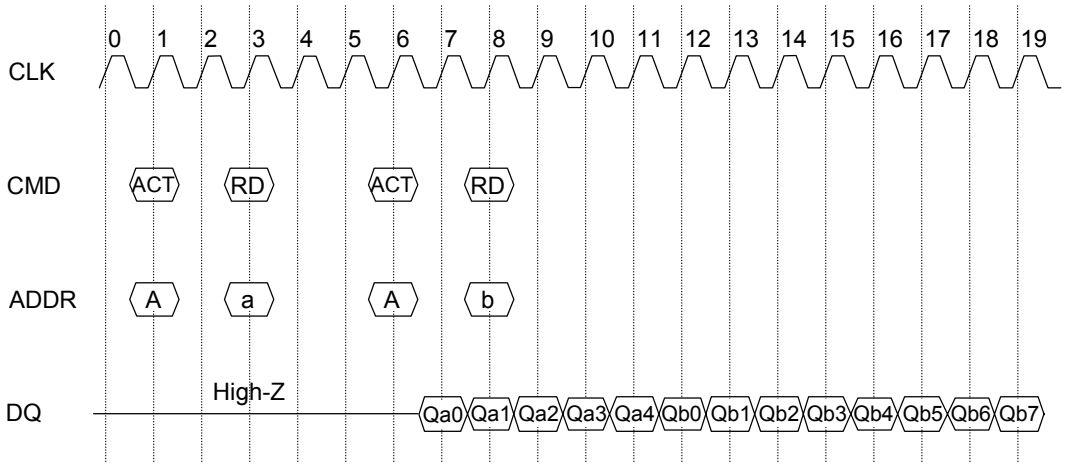
Burst Read/Interrupt II @ CAS Latency = 4, Burst length = 4



Preemptive Burst Read I @ CAS Latency = 4, Burst length = 8


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
CLK
CMD
RD RD RD RD
ADDR
a b c d
DQ
High-Z
Qa0 Qa1 Qa2 Qb0 Qb1 Qb2 Qb3 Qc0 Qc1 Qc2 Qc3 Qc4 Qd0 Qd1 Qd2

Preemptive Burst Read II @ CAS Latency = 4, Burst length = 8


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
CLK
CMD
ACT RD ACT RD
ADDR
A a A b
DQ
High-Z
Qa0 Qa1 Qa2 Qa3 Qa4 Qb0 Qb1 Qb2 Qb3 Qb4 Qb5 Qb6 Qb7

RECOMMENDED OPERATING CONDITIONS AND DC CHARACTERISTICS FOR PROGRAMMING (STO is High level)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	Notes
V_{PP} Supply Voltage	V_{PP1}	7.75	8.0	8.25	V	Program Mode	1
	V_{PP2}	–0.3	V_{CC}	V_{CC}+0.5	V	Read Mode	2
V_{CC} Supply Voltage	V_{CC1}	3.9	4.0	4.1	V	Program Mode	1
	V_{CC2}	4.5	4.6	4.7	V	Read Mode	2
	V_{CC3}	2.75	2.8	2.85	V	Read Mode	2
V_{PP} Current	I_{PP1}	—	—	50	mA	V_{PP} = 8.25 V, V_{CC} = 4.1 V	
	I_{PP2}	—	—	100	μA	V_{PP} = V_{CC} = 4.7 V	
V_{CC} Current	I_{CCP1}	—	—	150	mA	V_{PP} = 8.25 V, V_{CC} = 4.1 V	
	I_{CCP2}	—	—	200	mA	V_{PP} = V_{CC} = 4.6 V	
Input Leak Current	I_{IL}	–10	—	10	μA		
Output Leak Current	I_{OL}	–10	—	10	μA		
Output High Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = –400 μA	
Output Low Voltage Level	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA	
Input High Voltage	V_{IH}	3.2	—	V_{CC}+0.7	V	V_{CC} = 2.8/4.6 V	
Input Low Voltage	V_{IL}	–0.3	—	0.45	V	V_{CC} = 2.8/4.6 V	
Voltage Level on DC pin		–0.3	—	V_{CC}+0.5	V		
$\overline{OE}$ Input Distinctive High Voltage For Contact Check	V_H	6.6	6.7	6.8	V	V_{CC} = 3.0 V	
Operating Temperature	Ta	20	25	30	°C		

(Voltage levels are referred to V_{SS})

Notes:
1. Program represents the modes below.
   Program, Program Verify, Program Inhibit
2. Read represents the modes below.
   Read, Output Disable, Standby

FUNCTION TABLE FOR PROGRAMMING

	Function	V_{CC}	V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{WORD}$	DQ0~DQ15	CAP0~CAP8	Add.	$\overline{RAS}$ $\overline{CAS}$	AMPX	STO	Notes
Full Static	Program	4.0 V	8.0 V	L	H	L	D_{IN}	A0 to A8	A9 to A21	X	L/ Open	H	
	Program Inhibit	4.0 V	8.0 V	H	H	L	HZ	A0 to A8	A9 to A21	X	L/ Open	H	
	Program Verify	4.0 V	8.0 V	H	L	L	D_{OUT}	A0 to A8	A9 to A21	X	L/ Open	H	
	Read	2.8/ 4.6 V	2.8/ 4.6V	L	L	L	D_{OUT}	A0 to A8	A9 to A21	X	L/ Open	H	
	Output Disable	2.8/ 4.6 V	2.8/ 4.6V	L	H	L	HZ	A0 to A8	A9 to A21	X	L/ Open	H	
	Standby	2.8/ 4.6 V	2.8/ 4.6V	H	X	L	HZ	A0 to A8	A9 to A21	X	L/ Open	H	
	Contact Check	3.0 V	3.0 V	L	6.7 V	L	AAAA	0AA	16AA	X	L/ Open	H	1
	Contact Check	3.0 V	3.0 V	L	6.7 V	L	5555	155	0955	X	L/ Open	H	1
	Contact Check	3.0 V	3.0 V	L	6.7 V	L	5555	155	0955	X	L/ Open	H	1

ADDRESS MULTIPLEX

	Function	V_{CC}	V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{WORD}$	DQ0~DQ15	CAP0~CAP8	Add.	$\overline{RAS}$ $\overline{CAS}$	AMPX	STO	Notes
Address multiplex	Program	4.0 V	8.0 V	L	H	L	D_{IN}	-	-	H	H	H	
	Program Inhibit	4.0 V	8.0 V	H	H	L	HZ	-	RA/CA	↓	H	H	
	Program Verify	4.0 V	8.0 V	H	L	L	D_{OUT}	-	-	H	H	H	
	Read	2.8/ 4.6V	2.8/ 4.6V	L	L	L	D_{OUT}	-	RA/CA	↓	H	H	
	Output Disable	2.8/ 4.6V	2.8/ 4.6V	L	H	L	HZ	-	X	X	H	H	
	Standby	2.8/ 4.6V	2.8/ 4.6V	H	X	L	HZ	-	X	X	H	H	
	Contact Check	-	-	-	-	-	-	-	-	-	-	-	
	Contact Check	-	-	-	-	-	-	-	-	-	-	-	

(H = Logical high, L = Logical low, X = Don't Care in the range of logical level)

Notes:

1. Dual procedures to check complementary output codes on the indicated complementary address inputs assure every address, DQ, and $\overline{OE}$ pin connection.
   When address input code is incorrect, output code is "FFFF".

PROGRAMMING OPERATION

STO

Synchronous read is far different from anyone of conventional nonvolatile memories. STO input level switches operation mode either synchronous read or conventional EPROM/OTP type programming. The word "Programming" contains actual programming (inject electrons into floating gates of memory cells), program verify (verify data on actual programming bias), and read on programmer. High level STO assures full compatible programming operation with conventional EPROM/OTP. Low level STO assures high speed synchronous read. "Full static programming" is recommended for loose devices.

Program

MR27V6466F is programmed with 25 microsecond pulse width on 4.0 V V_{CC} and 8.0 V V_{PP}. OKI recommends consecutive programming, because of the similarity of device sorting process. Almost all words can be programmed sufficiently with one pulse. Programmers are recommended to be equipped with large current capacity of V_{PP} and V_{CC} supplying source and responsive capacitance (around 0.1 μF) on each socket to stabilize V_{PP} and V_{CC} voltage level, since switching speed of transistors produced with advanced wafer process technology is very fast and high voltage immunity of those is decreasing. Excessive overshooting of V_{PP} voltage may destroy device permanently. Excessive overshooting of V_{CC} voltage may cause misprogramming or disturbance. Excessive undershooting of V_{PP} or V_{CC} level may cause insufficient electron injection into floating gate. Additional programming increases programming time.

Program Inhibit

When V_{PP} is 8.0 V, address must be changed only in "Program Inhibit" mode.

Program Verify

This operation mode is utilized to check that each word is programmed sufficiently. It is recommended to take time more than some seconds between actual programming and "Program Verify" ("Read") for each word, because just after the actual programming (injection of electron into floating gate) of each word, pretended excessive electrons are attached around floating gate to show false sufficiency of programming. Programming flow is selected to separate "Program" and "Program Verify" to take enough time.

Contact Check

When programmed OTP lot contains failed devices at a rate of more than 0.1%, some of or almost all failed devices are caused by misconnection with the sockets on the programmer. The possibility of misconnection is increased with surface mount devices such as SOP or TSOP.
OKI will supply socket adapters exclusively applicable to MR27V6466F, but connections of all pins can not be assured with these socket adapters.
Following contact check sequence before actual programming is recommended.

1. Supply V_{CC} with 3.0 V power source.
2. Bias logical low level on $\overline{CE}$.
3. Supply 6.7 V on $\overline{OE}$ to enable contact check mode.
4. Apply two address codes and check each output respectively.
   If irregular address code is applied, then output is FFFF.
   <Connection of Address, D_{OUT}, V_{CC}, $\overline{OE}$, and STO pins are checked>
5. $\overline{CE}$ must be checked with a method suitable for the programmer.
6. V_{PP} can be checked with current flow (more than 100 μA) in Program Inhibit mode.
7. AMPX and $\overline{WORD}$ pins is open in the socket adapter, since these pins are pulled down to V_{SS} when STO is high.

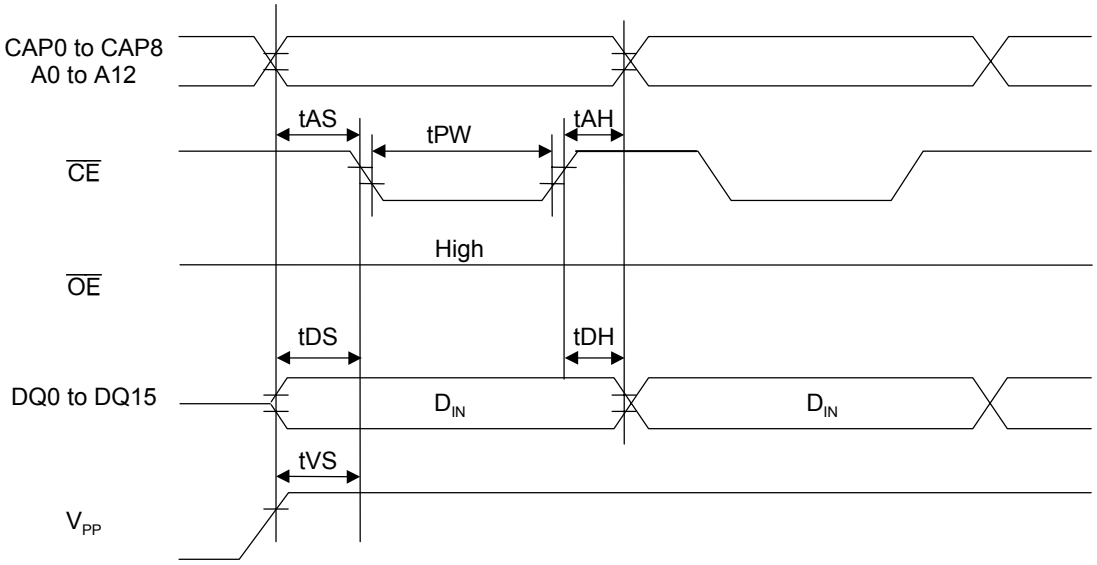
AC CHARACTERISTICS FOR PROGRAMMING (STO is High Level)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	Notes
V_{PP} Setup Time	tVS	2	—	—	µs	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Address Setup Time	tAS	100	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Data Setup Time	tDS	100	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Address Hold Time	tAH	1	—	—	µs	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Data Hold Time	tDH	100	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Program Pulse Width	tPW	24	25	26	µs	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
$\overline{OE}$ Setup Time	tOES	1	—	—	µs	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Data Valid from $\overline{OE}$	tOE	—	—	100	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
$\overline{OE}$ High to Output Float Delay	tOHZ	0	—	100	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Address Setup Time($\overline{RAS}$/$\overline{CAS}$)	tASR tASC	15	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
$\overline{RAS}$/$\overline{CAS}$ Pulse Width	tRAS tCAS	15	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Address Hold Time($\overline{RAS}$/$\overline{CAS}$)	tAHR tAHC	15	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
$\overline{RAS}$ Precharge Time	tRP	1	—	—	µs	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
$\overline{RAS}$ to $\overline{CAS}$ Delay	tRCD	30	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	
Address to $\overline{CE}$ Delay	tACD	100	—	—	ns	V_{PP} = 8.0 V, V_{CC} = 4.0 V	

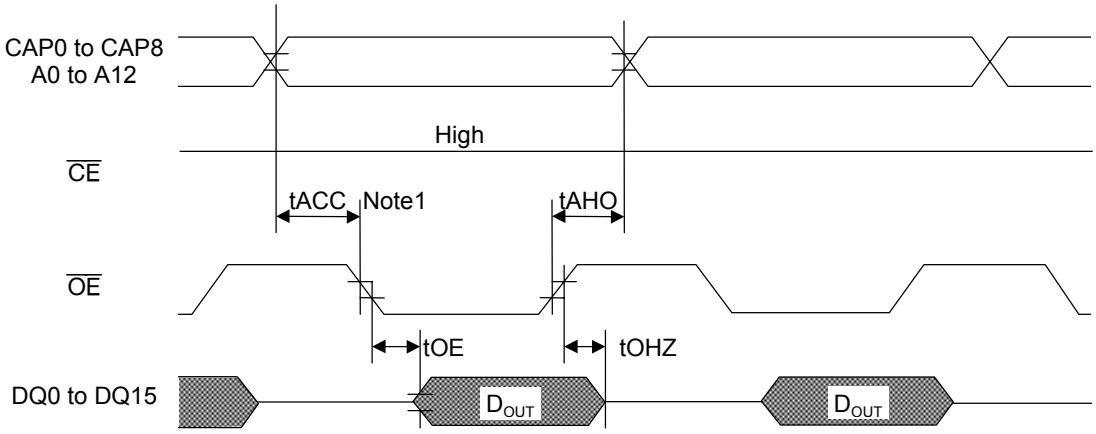
AC CHARACTERISTICS FOR VERIFY AND READ (STO is High Level)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	Notes
Address Access Time	tACC	—	—	100	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{RAS}$ Access Time	tACC	—	—	100	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{CAS}$ Access Time	tACC	—	—	100	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{CE}$ Access Time	tCE	—	—	100	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{OE}$ Access Time	tOE	—	—	30	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{CE}$ High to Output Float Delay	tCHZ	—	—	25	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{OE}$ High to Output Float Delay	tOHZ	—	—	20	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
Address Hold from $\overline{OE}$ high	tAHO	0	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
Address Setup Time($\overline{RAS}$/$\overline{CAS}$)	tASR tASC	15	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{RAS}$/$\overline{CAS}$ Pulse Width	tRAS tCAS	15	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
Address Hold Time($\overline{RAS}$/$\overline{CAS}$)	tAHR tAHC	15	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
$\overline{RAS}$ to $\overline{CAS}$ Delay	tRCD	30	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	
Address to $\overline{CE}$ Delay	tACD	100	—	—	ns	V_{PP} = V_{CC} = 2.8/4.6 V	

Consecutive Programming Waveforms (V_{PP} = 8.0 V, AMPX = L)



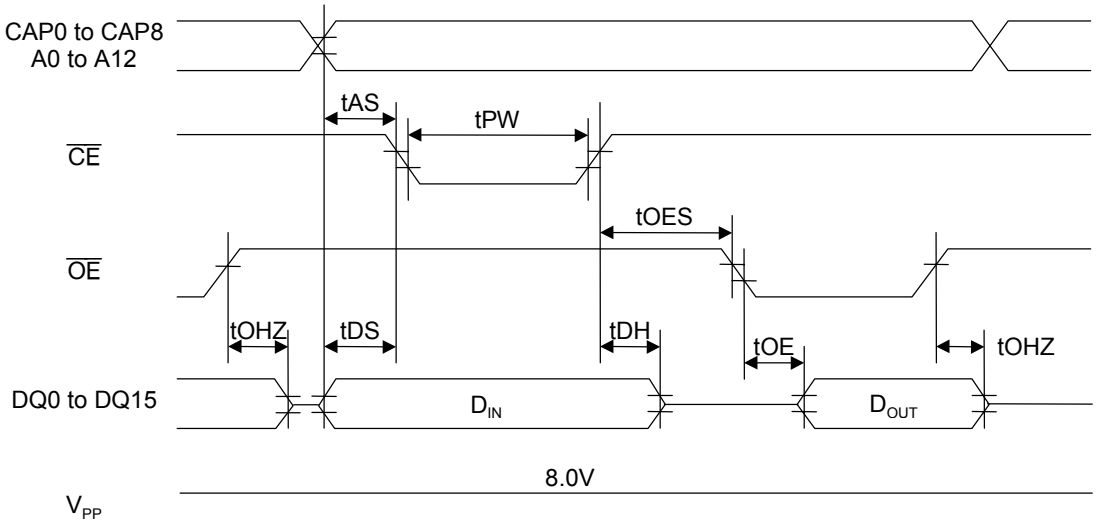
Consecutive Program Verify Cycle (V_{PP} = 8.0 V, AMPX = L)



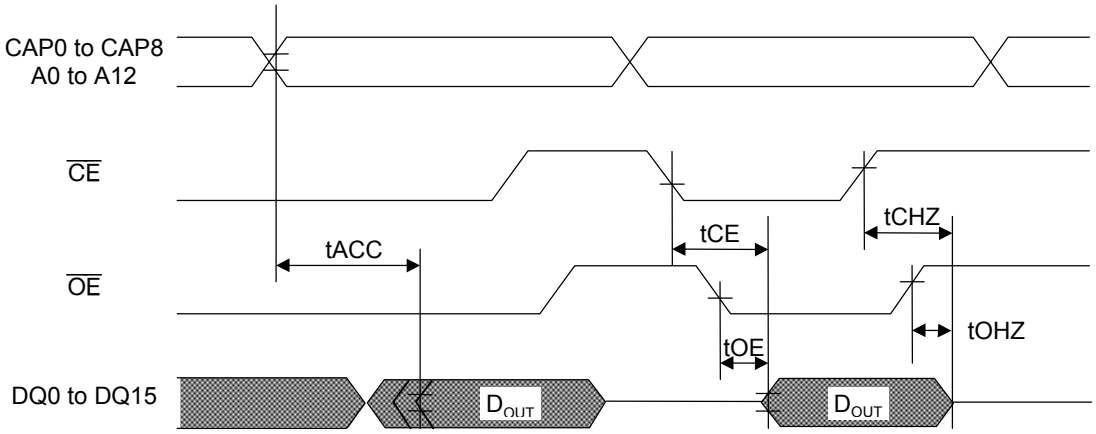
Notes:

1. Falling edge of $\overline{OE}$ must be preceded with data stabilizing time of more than tACC max, because output of invalid state can cause unstable system operation.
   Output buffer of MR27V6466F is designed to drive 100 pF load in 5ns.

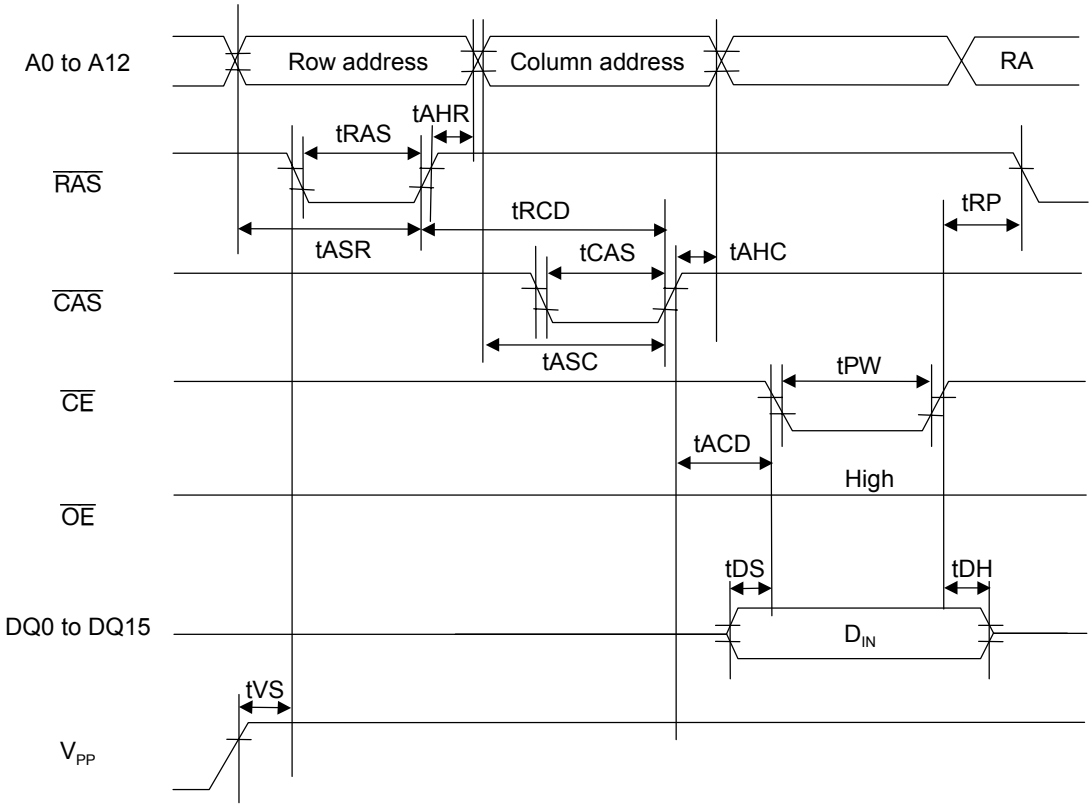
Program and Program Verify Cycle Waveforms (AMPX = L)



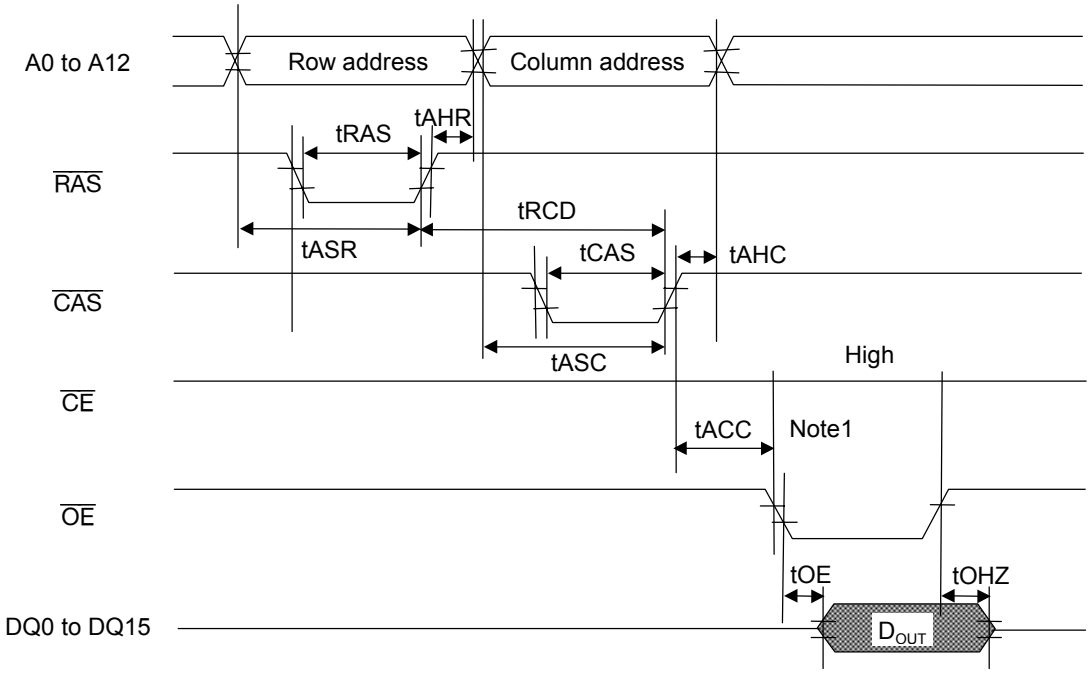
Read Cycle (AMPX = L)



Consecutive Programming Waveforms (V_{PP} = 8.0 V, AMPX = H, $\overline{WORD}$ = L)



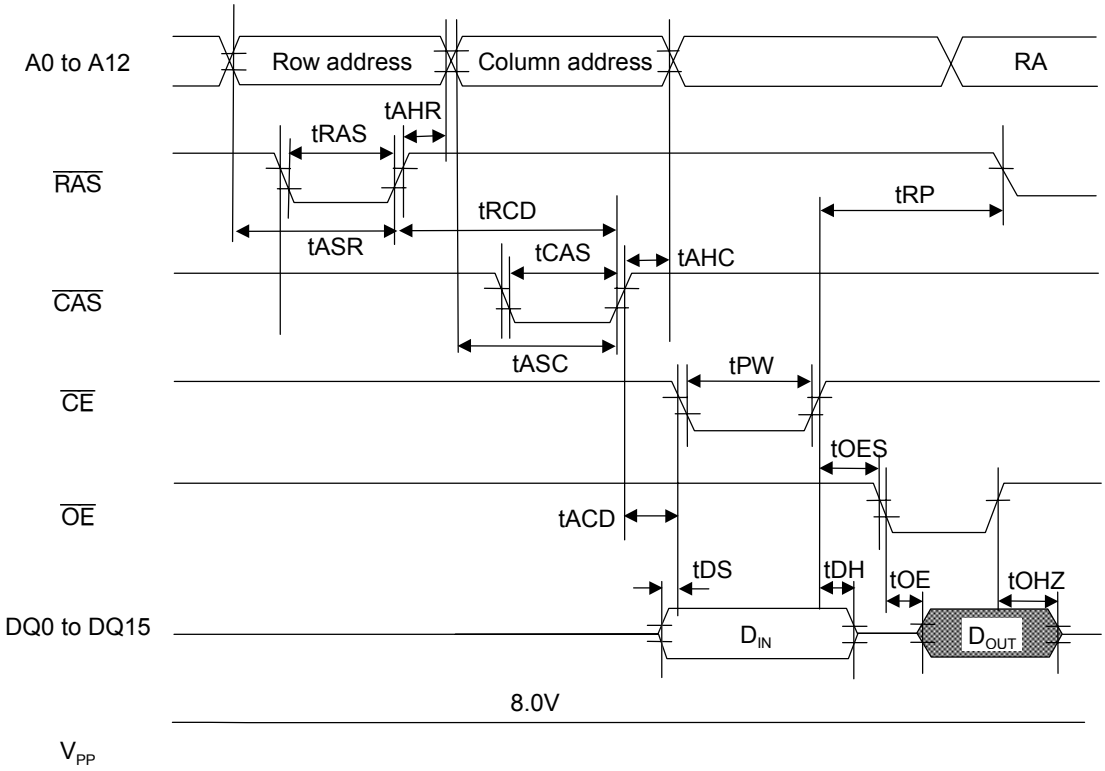
Consecutive Program Verify Cycle (V_{PP} = 8.0 V, AMPX = H, $\overline{WORD}$ = L)



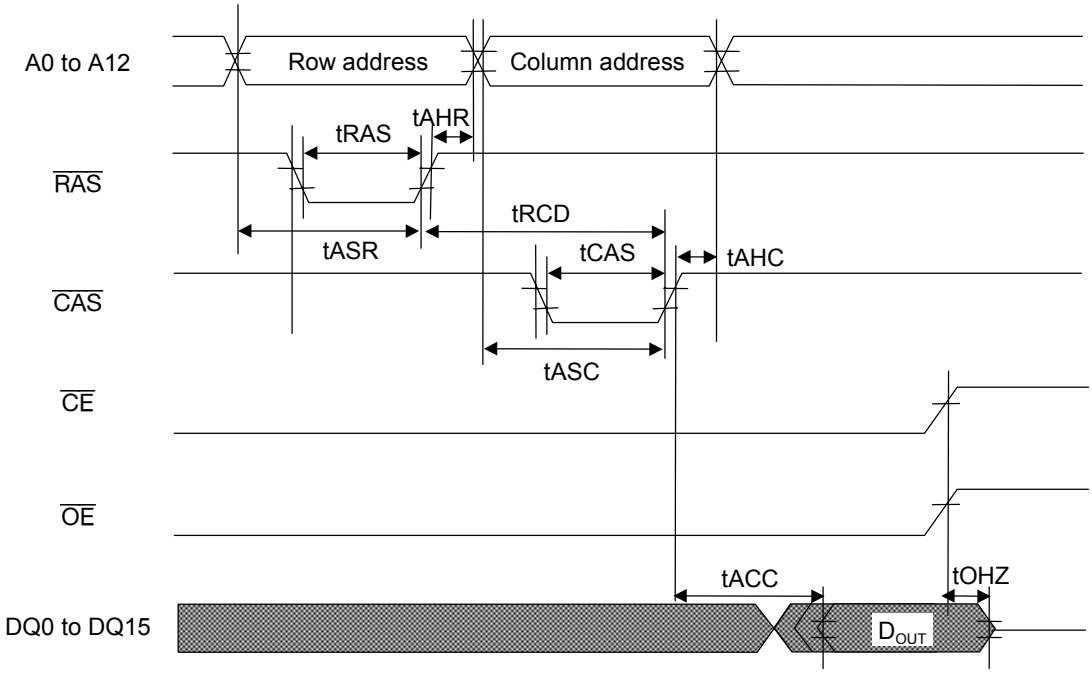
Notes:

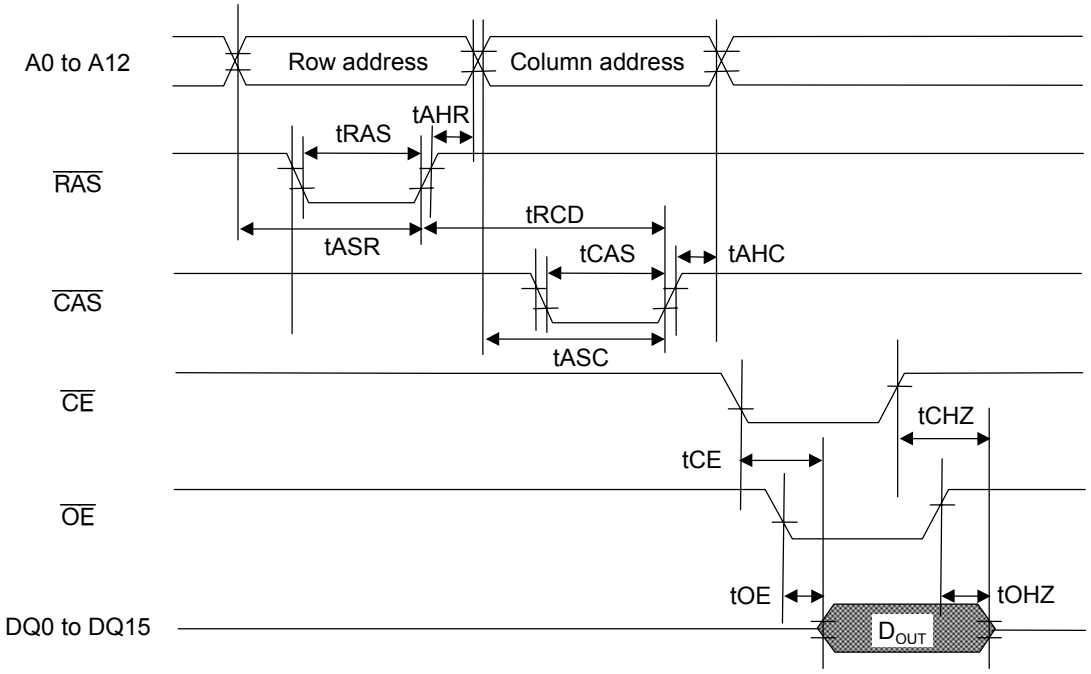
1. Falling edge of $\overline{OE}$ must be preceded with data stabilizing time of more than tACC max, because output of invalid state can cause unstable system operation.
   Output buffer of MR27V6466F is designed to drive 100 pF load in 5ns.

Program and Program Verify Cycle Waveforms (AMPX = H, $\overline{WORD}$ = L)

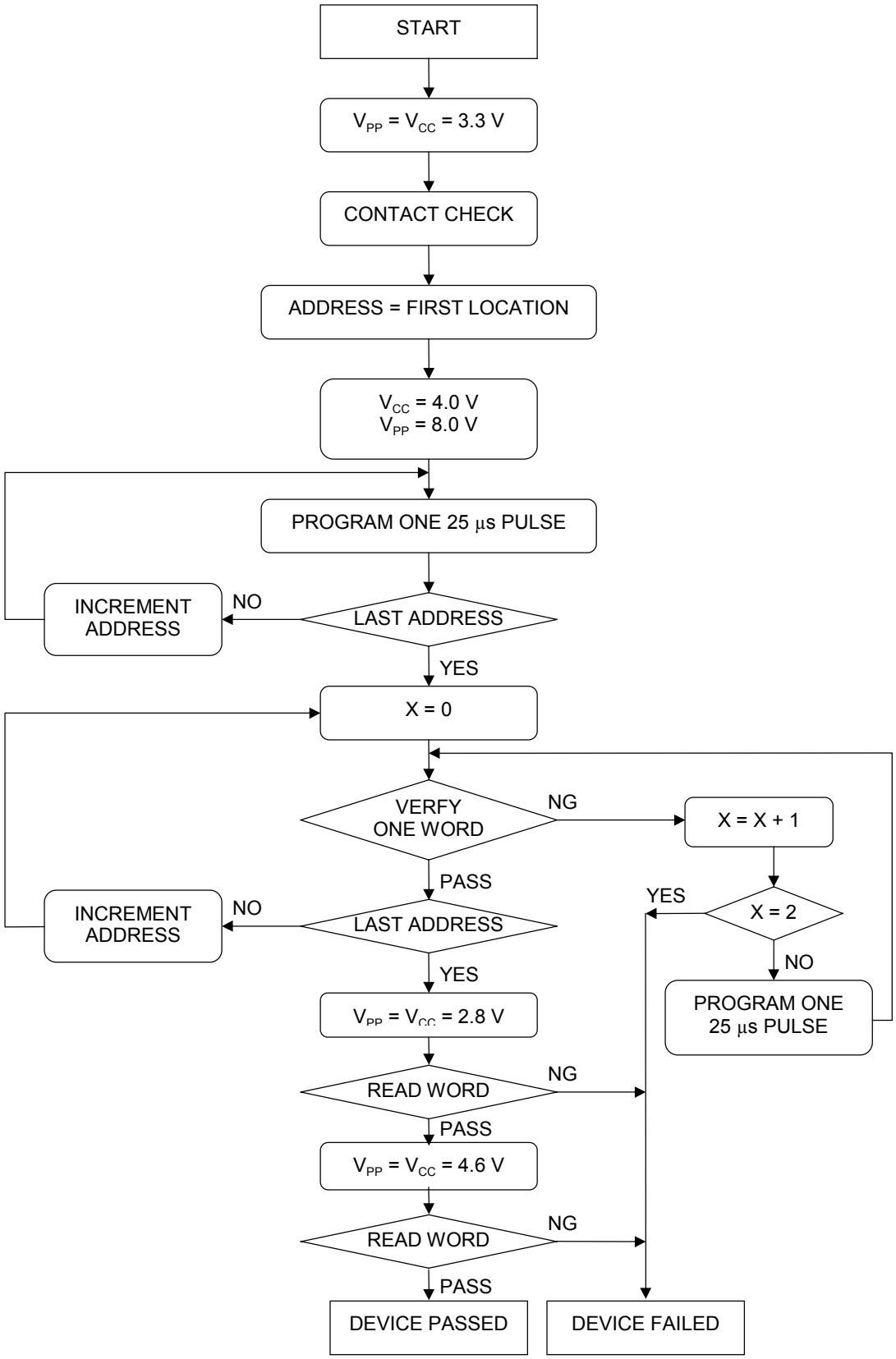


Read Cycle (AMPX = H, $\overline{WORD}$ = L)





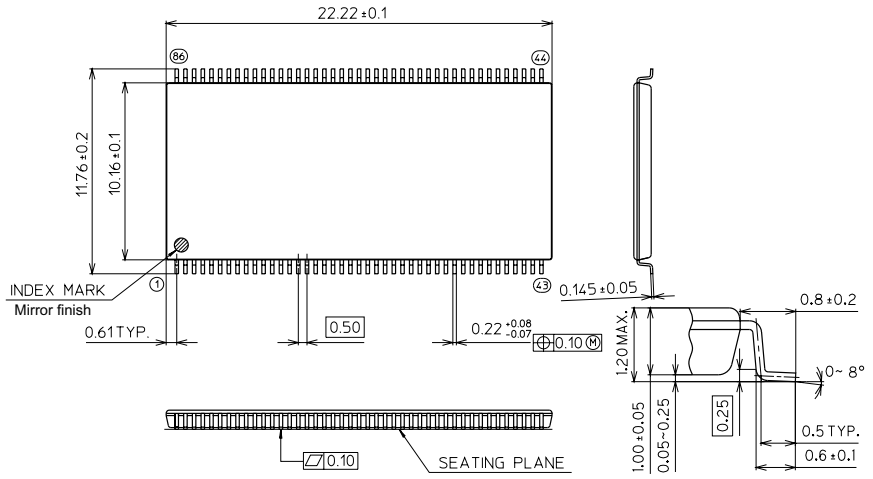
PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

(Unit: mm)

TSOP(2)86-P-400-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.53 TYP.
Rev. No./Last Revised	1/Jul. 14, 1998

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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